

Investigation of Low-Energy Tilted Ion Implantation for FinFET Extension Doping

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1. Introduction

One of the most important issues in the high-performance FinFET fabrication is the reduction of parasitic source-drain (SD) resistance (R_p) that is mainly determined by the narrow fin extension [1]. For reducing the R_p , highly tilted angle and low-energy ion implantation (I/I) has been used to introduce impurities into the fin extension effectively [2-5]. However, the highly tilted I/I technique becomes difficult with shrinking device size owing to the ion shadowing by adjacent fins or photoresist edges [3, 4]. In the case of a low tilted angle I/I, on the other hand, the implant atoms easily scatter out from the fin extension regions [6], which results in the dopant loss. Hence, the optimization of fin extension I/I process is strongly required.

In this paper, the $I_{ON-IOFF}$ and R_p of the n^+ -poly-Si gate n-channel FinFETs fabricated by changing extension I/I conditions including dose (D) and tilt angle (θ) are systematically compared and discussed.

2. Experimental results and discussion

Si-fin channels were fabricated by using the orientation-dependent wet etching on the (110) SOI wafers [7]. The n^+ -poly-Si gate length (L_g) was ranged from 50-175 nm. In the I/I process, arsenic (As) for fin extension with a fixed low-energy of 5-keV and phosphorus (P) for SD electrodes are used as shown in Fig. 1. For impurity activation, RTA was performed at 900 °C for 2 s. An ideal rectangular Si-fin channel is confirmed from the STEM image as shown in Fig. 2.

At first, we evaluated the $I_{ON-IOFF}$ at a fixed $V_d = 1$ V. Since the actual V_{th} is around -0.2 V as shown in Fig. 3(a), in the evaluation of the $I_{ON-IOFF}$, the V_g range is shifted to the negative direction by 0.4 V. Next, we evaluated the R_p by using the Terada's method [8] and by its modified implementation [1]. Figure 3(b) shows the on-state resistance ($R_{ON} = V_d/I_d$) at $V_d = 0.05$ V. The y-intercepts provide the R_p at a given gate overdrive. We chose $V_g - V_{th} = 0.6$ V, and extracted the R_p for all devices. The I_{ON} , I_{OFF} and R_p were normalized by $2H_{fin}$.

Figures 4(a) and 4(b) show the measured $I_{ON-IOFF}$ and R_p for the devices by changing θ from 0 to 60°. It is clear from Fig. 4(a) that the I_{ON} increases with increasing θ , indicating the superiority of the highly tilted angle I/I. Somewhat lower I_{ON} and marked fluctuation in I_{OFF} and R_p are observed at $\theta = 0^\circ$, which will be discussed later.

Figures 5(a) and 5(b) show the measured $I_{ON-IOFF}$ and R_p for the devices by changing D from $1E14$ to $8E14$ cm⁻². Note that the best $I_{ON-IOFF}$ performance and lowest R_p are obtained when the D is chosen to be $4E14$ cm⁻². In the case of lower D of $1E14$ cm⁻², the total impurities introduced into the fin extension regions should be smaller than those in the case of $D = 4E14$ cm⁻², which reasonably results in a

higher R_p . On the other hand, with further increasing D , in contrast, the $I_{ON-IOFF}$ and R_p are deteriorated. It is speculated that the $D = 8E14$ cm⁻² is high enough to cause amorphization, and the re-crystallization of the defected amorphous fin extension is insufficient, which results in the poor impurity activation and fluctuations in $I_{ON-IOFF}$ and R_p [5].

Figures 6(a) and 6(b) show the measured $I_{ON-IOFF}$ and R_p for the devices by changing D from $4E14$ to $1.07E15$ cm⁻². It should be noted that the $D = 1.07E15$ cm⁻² at $\theta = 0^\circ$ is chosen so that the implanted impurities to the extension regions are equivalent to that in the case of $D = 4E14$ cm⁻² at $\theta = 60^\circ$. Note that no performance improvement is observed even if D increases to $1.07E15$ cm⁻², and the R_p fluctuation is enhanced compared with that in the case of $D = 4E14$ cm⁻² at $\theta = 60^\circ$. This result implies that the implanted atoms scatter out from the upright thin fin extensions randomly [6]. As a result, the net impurities remained in the fin extension regions are different each other, which result in the marked fluctuations in R_p as shown in Fig. 6(b).

Figure 7 summarizes the θ dependence of average R_p at a fixed $D = 4E14$ cm⁻². The smallest R_p is obtained to be 0.64 k Ω - μ m when the I/I condition is chosen to be $D = 4E14$ cm⁻² & $\theta = 60^\circ$. This value is comparable with the $R_p = 0.53$ k Ω - μ m by the solid-phase-diffusion of phosphors from PSG, which is conformal and damage-free process [7]. This indicates that above I/I condition is almost optimized.

3. Conclusion

The low-energy tilted I/I for FinFET source-drain extension doping has been investigated thoroughly by fabricating a series of n^+ -poly-Si gate n-channel FinFETs with different I/I conditions. It is experimentally found that the best extension I/I condition is $D = 4E14$ cm⁻² & $\theta = 60^\circ$. With further increasing D , the device performance deteriorates due to the incomplete re-crystallization of amorphous regions in the fin extensions. In the case of $\theta = 0^\circ$, the marked increment and fluctuations in R_p are observed owing to the implant atoms scattering out randomly from each fin extension.

Acknowledgements

This work was supported in part by the Innovation Research Project on Nanoelectronics Materials and Structures of METI, Japan. The authors would like thank Dr. T. Yoshida and Dr. M. Nagao for their help in the I/I process.

References

- [1] T. Matsukawa, et al., IEEE SOI Conf. Dig. (2008) 159.
- [2] K. Endo, et al., IEDM Tech. Dig. (2008) 857.
- [3] A. Nackaerts, et al., IEDM Tech. Dig. (2004) 269.
- [4] H. Kawasaki, et al., IEDM Tech. Dig. (2008) 237.
- [5] R. Duffy, et al., ESSDERC Tech. Dig. (2008) 334.
- [6] M. Masahara, et al., Jpn. J. Appl. Phys., 44, (2005) 2400.
- [7] Y. X. Liu, et al., IEEE EDL, 24, (2003) 484.
- [8] K. Terada, et al., Jpn. J. Appl. Phys., 18, (1979) 953.

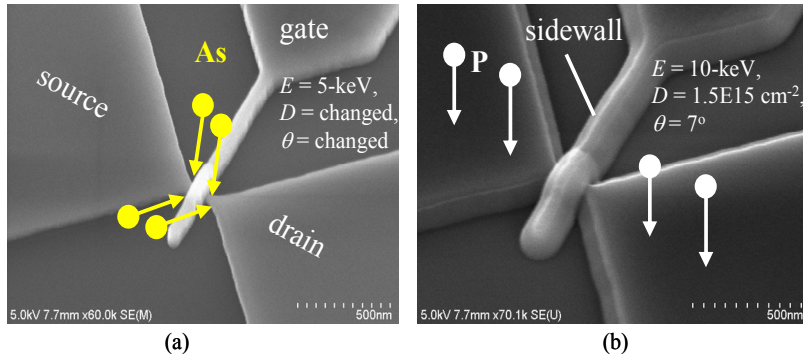


Fig. 1. SEM images of the fabricated FinFETs after (a) n⁺-poly-Si gate formation by ICP-RIE and (b) sidewall spacer formation. In the I/I process, arsenic (As) for extension with a fixed low-energy of $E = 5$ -keV and phosphorus (P) for source-drain electrodes are used.

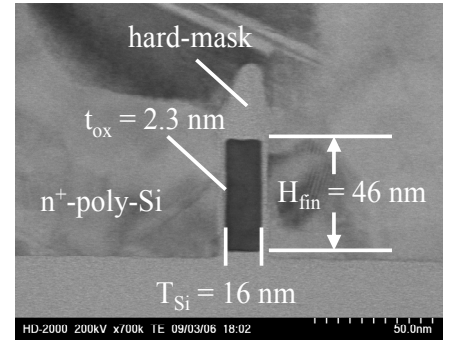


Fig. 2. Cross-sectional STEM image of the fabricated n⁺-poly-Si gate FinFET by using the orientation-dependent wet etching.

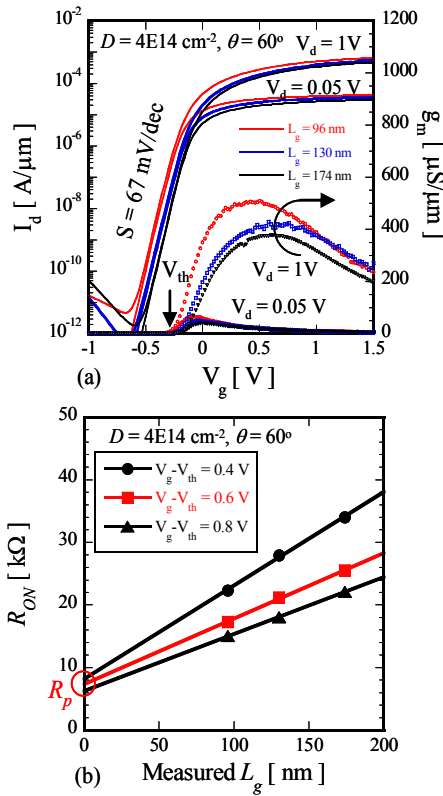


Fig. 3. (a) I_d - V_g & g_m - V_g (b) R_{ON} - L_g characteristics of the fabricated FinFETs.

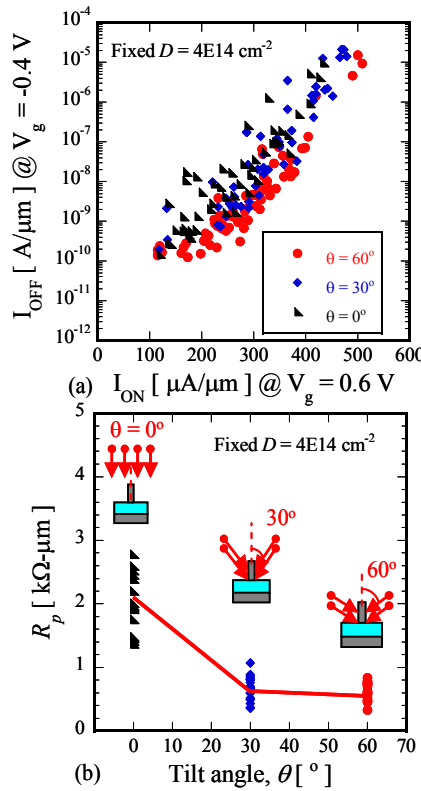


Fig. 4. (a) I_{ON} - I_{OFF} plot at $V_d = 1$ V and (b) normalized R_p as a function of θ .

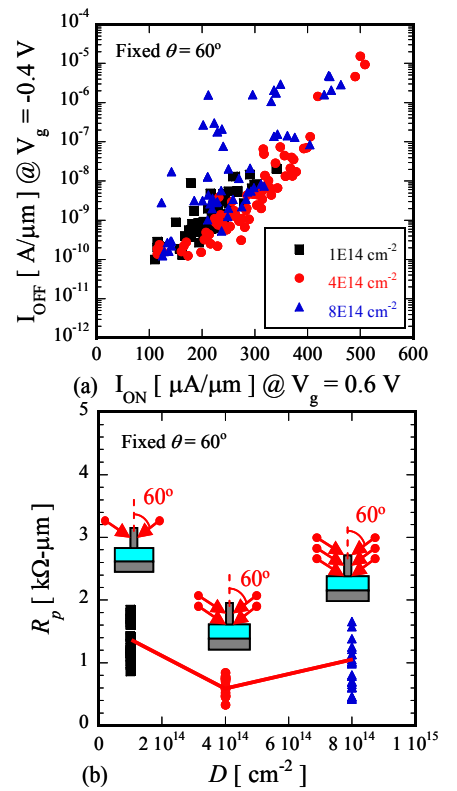


Fig. 5. (a) I_{ON} - I_{OFF} plot at $V_d = 1$ V and (b) normalized R_p as a function of I/I dose.

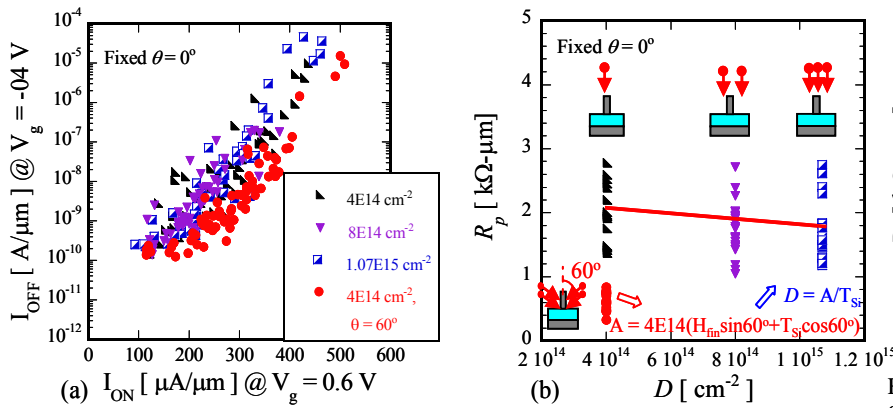


Fig. 6. (a) I_{ON} - I_{OFF} plot at $V_d = 1$ V and (b) normalized R_p as a function of I/I dose at a fixed $\theta = 0^\circ$. Data for $D = 4E14$ cm⁻² & $\theta = 60^\circ$ are also plotted for comparison.

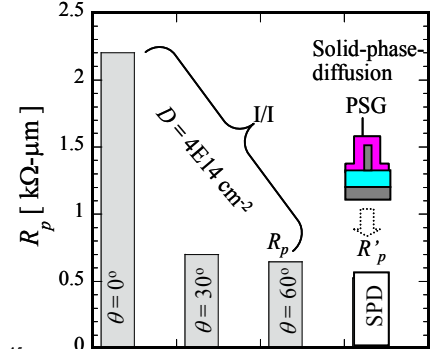


Fig. 7. Summary of average R_p values at a fixed dose of $D = 4E14$ cm⁻² with the θ as a parameter. The R'_p by solid-phase-diffusion (SPD) from PSG is also plotted for comparison.