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Random-Dopant-Induced Static Noise Margin Fluctuation and Suppression in 16-nm-Gate CMOS SRAM Cell

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1. Introduction

Intrinsic parameter fluctuation is crucial for design window, reliability and yield of nanoscale CMOS circuits [1-4]. In this study, 3D "atomistic" coupled device-circuit simulation is intensively performed to explore the impact of random-dopant-fluctuation (RDF) on static noise margin (SNM) of 16 nm CMOS SRAM cell. Fluctuation suppression based on circuit and device viewpoints are implemented to examine the associated characteristics; from the circuit viewpoint, an 8T planar SRAM architecture is advanced for high SNM and low SNM fluctuation (σ_{SNM}). To prevent the increase of chip area, doping profile engineering and the use of SOI FinFETs to replace the planar CMOS in 6T SRAM are further examined.

2. Methodology and Results

All explored devices are with 1.48×10^{18} cm^{-3} nominal channel doping concentrations. Threshold voltage (V_{th}) of 65-nm-gate MOSFET is calibrated to 280 mV for studying the roll-off characteristics of SNM and σ_{SNM}. For RDF, to consider the randomness of the number and position of discrete channel dopants, 50806 dopants are randomly generated in a large cube (325 nm x 325 nm x 325 nm), in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 1(a). The large cube is then partitioned into 125 sub-cubes of (65 nm x 65 nm x 65 nm). The number of dopants may vary from 70 to 130, and the average number is 100, as shown in Figs. 1(b) and 1(c), respectively. These sub-cubes are equivalently mapped into the device channel for the 3D "atomistic" device simulation with discrete dopants, as shown in Fig. 1(d). Similarly, we can generate the sets of discrete dopant cases for the 32-nm- and 16-nm-gate devices, as shown in Figs. 1(e) and 1(f), respectively. We also apply the statistical approach to evaluate the effect of process variation effect (PVE), following the projections of the ITRS 2007. Figures 1(g) and 1(h) illustrate the explored 6T and 8T SRAM cells, respectively.

Figures 2(a) and 2(b) show the roll-off characteristics for V_{th} and SNM for 65-nm- to 16-nm-gate devices, respectively. The error bars are the RDF- and PVE-induced V_{th} fluctuation (σV_{th}) and σ_{SNM} for each corresponding technology node. As the gate length scales from 65 nm to 16 nm, the total σV_{th} increases significantly from 16 mV to 64 mV. The RDF plays the major source of fluctuation and may induce two to four times larger fluctuation than the PVE. The σV_{th} of 16 nm MOSFET is around 4 times larger than that of 65 nm, which follows the trend of the analytical model [5]. For SNM and σ_{SNM}, as gate length scales from 65 nm to 16 nm, the SNM decreases significantly from 138 mV to 20 mV. The normalized σ_{SNM} of 16-nm-gate device with V_{th}=140 mV is 80%. Figure 3(a) summarized the normalized σ_{SNM} for the explored SRAM. To confirm the simulation accuracy for circuit characteristic fluctuations and find out the most sensitive components in SRAM, the transistors in a 6T 16-nm-gate SRAM are classified into driver, access, and load transistor and then analyzed. Figure 3(b) shows the sensitivity of SRAM by investigating the RDF in different transistor pairs. The access transistors contribute the largest SNM fluctuations because the stored data was read out through the access transistors during the read operation. Since the influences of each transistor pairs on total SNM fluctuation ($\sigma_{SNM\text{-}Total}$) are independent, the relationship between $\sigma_{SNM\text{-}Total}$ and its components can be expressed as following:

$$(\sigma_{SNM-Total})^2 \cong (\sigma_{SNM-Driver})^2 + (\sigma_{SNM-Access})^2 + (\sigma_{SNM-Load})^2, \qquad (1)$$

where $\sigma_{SNM\text{-}Driver}$, $\sigma_{SNM\text{-}Access}$, and $\sigma_{SNM\text{-}Load}$ are σ_{SNM} induced by driver, access, and load transistors, respectively. The $\sigma_{SNM\text{-}Total}$ from the summation of different transistor pair induced SNM fluctuation is 36 mV, which shows a good agreement to the result obtaining from all transistor with totally random fluctuation, 38 mV. The simulation accuracy for circuit characteristic fluctuations is therefore confirmed.

Due to the worse operation characteristics for 6T planar SRAM with V_{th}=140 mV, various improvement and suppression approaches based on the circuit and device viewpoints are implemented to examine the associated characteristics in 16-nm-gate SRAM cells. From the circuit viewpoint, an 8T planar SRAM architecture is first explored [6]. Figure 4(a) shows the static transfer characteristics of 8T SRAM cells including RDF-fluctuated cases, where the device V_{th} is 140 mV. The dashed lines illustrated RDF and PVE fluctuated cases, and the solid line is the nominal case. Due to the separation of data access element, the influence result from bit-line is reduced and increased the nominal SNM to 233 mV. The RDF induced SNM fluctuation is 22 mV, which is less than 10% variation. Comparing with original planar 6T SRAM cell, the nominal SNM is 12 times larger and normalized RDF induced SNM fluctuation is suppressed by a factor of 8.4. Notably, thought the 8T SRAM can enlarge the SNM and reduced the SNM fluctuation, the chip area is increased by 30%. Notably, the 6T SRAM with cell ratio equal to two also require 30% extra area; however, the nominal SNM is 92 mV, which is not enough for proper circuit operation and therefore will not be discuss herein.

Figure 4(b) present the sensitivity of SNM fluctuation of 8T SRAM cell, where the impact of access transistors is significantly reduced due to the read operation is not performed through these two transistors in 8T structure and the driver transistors become the dominating factor of the SNM fluctuation. To further suppress the RDF induced SNM fluctuation, vertical doping profile engineering, as shown in Fig. 5(a), has been implemented to reduce the RDF-induced fluctuations in planar SRAM cells with high V_{th}. Figure 5(b) shows the static transfer characteristics of 16 nm planar SRAM with higher V_{th} devices with vertical doping profile. The vertical doping profile engineering can further suppress RDF induced SNM fluctuation from 41.7 mV to 30.5 mV; however, it may also suffer from more serious short channel effect (SCE), which reduces the SNM to 71 mV. Additionally, the PVE-induced SNM fluctuation is increased from 18 mV to 24.4 mV. To alleviate this point, based on the same layout area as 16-nm-gate planar MOSFETs, a 16-nm-gate SOI FinFETs as shown in Fig. 6(a) is then adopted to replace the planar MOSFETs to examine associated fluctuation resistivity against RDF and PVE. Without loss of generality, the equivalent doping concentration is 1.48×10^{18} cm^{-3} and the nominal V_{th} of SOI FinFETs is 140 mV. The number of dopants in a sub-cube may vary from 2 to 24, and the average is 13, as shown in Fig. 6(a). Figure 6(b) shows static transfer characteristics of 16 nm SOI FinFET SRAM cells, where the inset presents the RDF and PVE induced σ_{SNM}. Comparing with the original case, the SNM of 6T SOI FinFETs SRAM is 125 mV and the σ_{SNM} is suppressed significantly to 5.4 mV (4.3% normalized σ_{SNM}).

3. Conclusions

Figure 7 summarized different improvement techniques. From the circuit viewpoint, an 8T planar SRAM architecture is explored whose SNM is enlarged to 230 mV and the σ_{SNM} is reduced to 22 mV (around 9.6% normalized σ_{SNM}) at a cost of 30% extra chip area. To prevent the increase of chip area, silicon-on-insulator SOI FinFETs replaced the planar MOSFETs in 6T SRAM is further examined. The SNM of 6T SOI FinFETs SRAM is 125 mV and the σ_{SNM} is suppressed significantly to 5.4 mV (4.3% normalized σ_{SNM}). The 8T SRAM architecture can provide largest SNM and is promising in near future design; however, to prevent the increase of chip area and suppress the intrinsic parameter fluctuations, development of fabrication for SOI FinFET SRAM is crucial for sub-22nm technology era.

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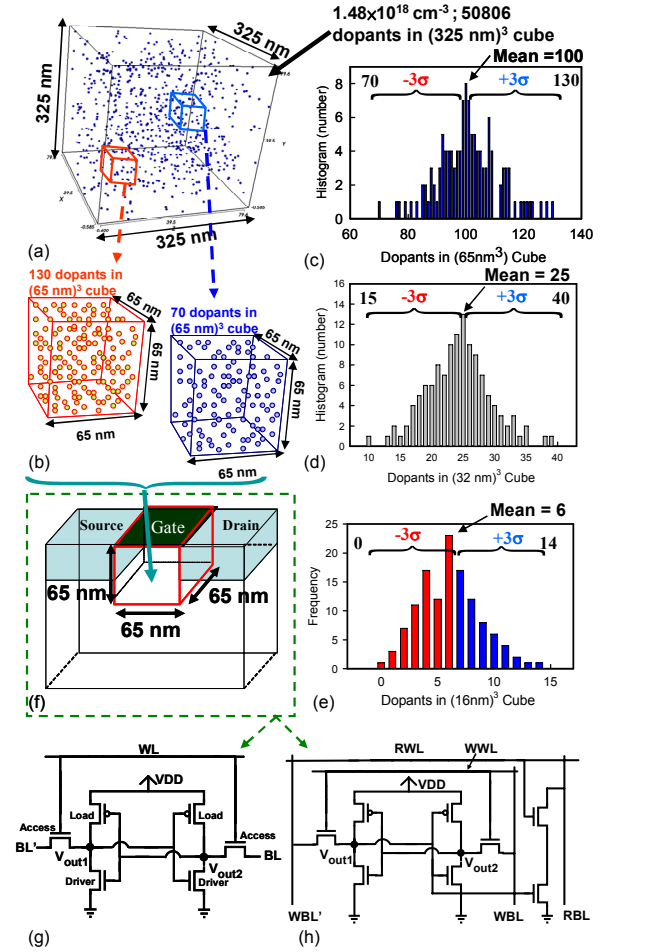

Figure 1. (a) Discrete dopants randomly distributed in the large cube with the average concentration of 1.48×10^{18} cm^{-3}. There will be 50806 dopants within the cube, for 16 nm gate devices, dopants may vary from 70 to 130 (average is 100), within its sub cubes of 65 nm × 65 nm × 65 nm, [(b), (c)]. The sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in MOSFET (e). The dopants may vary from 15 to 40 (average = 25) for 32 nm gate devices (f) and 0 to 14 (average = 6) for 16-nm-gate devices (g). The schematics of (g) 6T and (h) 8T SRAM cells.

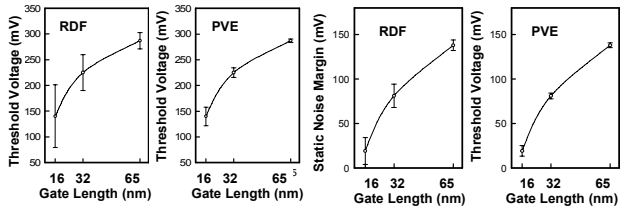

Figure 2. (a)V_{th} and (b) SNM fluctuations induced by RDF and PVE for different gate lengths of planar MOSFETs.

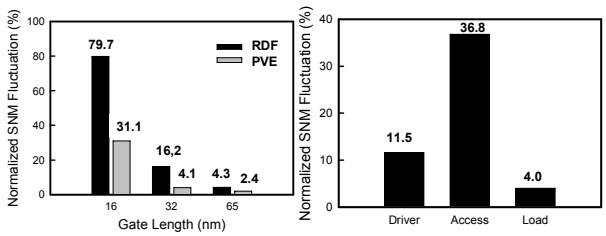

Figure 3. (a) SNM fluctuations induced by RDF and PVE for different gate lengths of SRAM cells. (b) The influence of different transistor pairs on total SNM fluctuation of planar 6T SRAM cell.

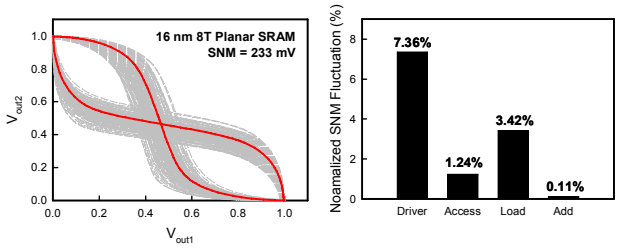

Figure 4. (a) Static transfer characteristics of planar 8T SRAM cells. (b) The influence of different transistor pairs on total SNM fluctuation of planar 8T SRAM cell.

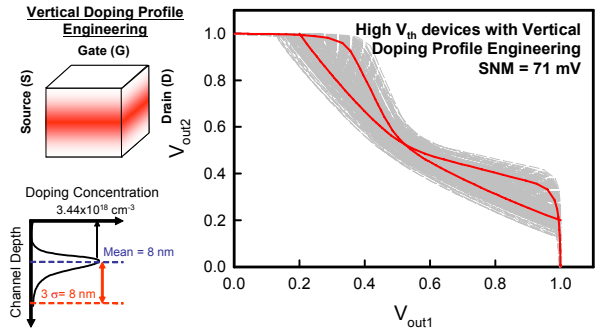

Figure 5. (a) Illustration of doping profile engineering. (b) Static transfer characteristics of improved 6T SRAM cells, the threshold voltage of devices were raised to 350 mV.

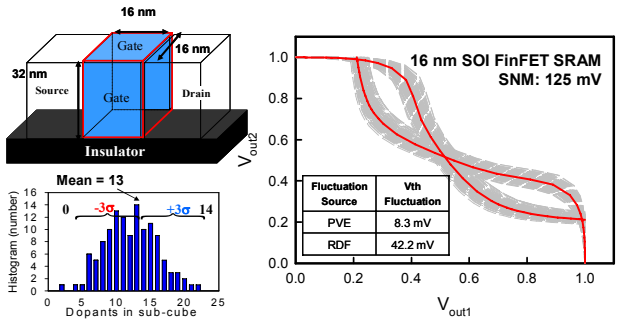

Figure 6. (a) The explored SOI FinFET structure and distribution of generated discrete dopant cases. (b) Nominal and fluctuated static transfer characteristics of 16 nm SOI FinFET SRAM cells.

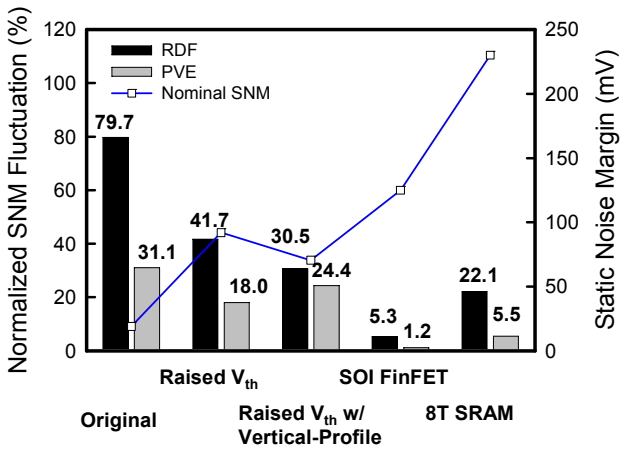

Figure 7. Summary of intrinsic-parameter-fluctuation-induced SNM and SNM fluctuation for different improvement techniques.