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Through-Si-Via Technology Solutions for 3D System Integration

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1. Introduction

Through Silicon Vias (TSVs) are an enabler for 3D system integration. A wide diversity of technologies is being proposed. Different application domains have different TSV requirements and justify different integration approaches. Key technologies are discussed for the TSV realization in the wafer fab (via-middle, 3D-SIC) or post process realization of TSV connections (via-last, 3D-WLP).[1-3]

3D system integration requires several novel technology steps. Not only for the TSV processing itself, but also for the wafer thinning, thin wafer handling and die stacking and stack packaging. Also these aspects are discussed.

2. 3D-WLP, post-processes TSV processing

Post-processed TSV technologies typically require lengthy Si-etch and metal fill process steps. In order to obtain a cost effective TSV process, the TSV volume must be minimized. This can be done by scaling down the via diameter or thinning the Si wafer. Practically this requires a higher aspect ratio via. For aspect ratio's (Si thickness/diameter via) below 2-3 standard PVD techniques can be used to deposit the barrier metals and seed layers. Higher AR's, up to 5 and even 10 can still be done with enhanced sputtering tools at a higher cost of ownership. Very high AR's require CVD processes for metallic seed deposition. Therefore in order to have a cost effective process for 3D-WLP TSV structures, a low AR has to be maintained, typically between 1:1 and 3:1.

The IMEC approach to a 3D-WLP TSV's is to realize the TSV from the wafer backside and contact to the first metal layer of the die interconnect stack. This requires to first bond the wafers to a temporary carrier wafer, followed by wafer thinning down to 100 or 50 µm.

For large diameter TSV structures in 100 µm thick Si wafers, plating times for fully filled TSV's may approach 3 hours per wafer, resulting in an uneconomical process. In that case, it is preferable to use a conformal Cu-plating in an open TSV structure as shown in figure 1.[4] This conformal Cu-TSV is however not scalable to very tight interconnect pitches. For the higher density 3D-WLP TSV structures, a fully filled TSV structure is required. As the plating time is a critical factor in the overall TSV process cost, a 50µm thick Si-wafer is used. For the larger aspect ratio 3D-WLP TSV, we then etch a 5 µm wide circular trench, "donut", in the Si, stopping at the front side oxide layer. This circular trench is filled with a polymer dielectric using a spin-coating technique. The polymer layer is opened on top of the Si-center of the (polymer) donut. This allows for the selective (wet or dry) etching of the central Si pillar and the back-etching of the oxide at the bottom of the hole, exposing the metal contact pad. The final steps are the PVD deposition of a barrier and Cu seed layer, followed by the electroplating of the Cu via. An important advantage over the sloped via process is that no lithography at the bottom of the via is required. Examples of such 3D-WLP TSV's are shown in figure 1.

3. 3D-SIC, TSV processing during device fabrication

For 3D-SIC smaller diameter and pitch TSV structures are used. Our approach to 3D-SIC stacking, consists of realizing the Cu TSV, so-called "Cu-nail", during the IC process.[6-8] This Cu-nail is processed after the FEOL process (transistors), but before the BEOL process (multilayer damascene interconnect layers), as shown in figure 2.

In our current process, the Cu-nail diameter is 5 µm. The via hole is etched using a Bosch-type recipe down a Si-depth of 25µm (aspect ratio 5:1) or 50 µm (aspect ratio 10:1). A SACVD O3-TEOS oxide layer is used as thin dielectric insulating layer. A Ta metal barrier and Cu seed is then deposited by PVD. This process step is probably the most critical step with respect to the achievable aspect ratio of the via. In particular the barrier layer has to be continuous down to the bottom of the via. This requires advanced ionized PVD technologies. Subsequently, the via hole is filled with electroplated copper. CMP is used to remove the Cu "overburden". In figure 2, 3D-SIC TSV's are shown after completing this CMP step. After this process, standard BEOL is used to finalize the Si-die.

4. Wafer thinning and thin wafer handling

Both for 3D-WLP and 3D-SIC TSV technology wafer thinning and processing on thin wafers is required. Many approaches to wafer thinning and die singulation have been developed for traditional die-stacking approaches. These are however not readily applicable for TSV technologies. The main limitations are the temperature stability, cleanliness and compatibility with standard semiconductor equipment.

The most prominent approaches are the use of a thermoplastic polymer glue layer that can be debonded by mechanically 'sliding-off' the carrier wafer from the device wafer, the use of a laser through glass carriers to debond polymer glue layers, the use of mechanically 'peelable' glue layers and the use of electrostatic bonded carriers

5. 3D-stacking

The stacking of high density TSV structures requires fine pitch chip-to-chip interconnects. For the 3D-WLP TSV technology and for the coarser pitch 3D-SIC technologies, a Cu-Sn based micro bump is used. Typically a 3µm thick Cu and 2µm thick Sn layer are used. This bump is bonded to a slightly larger Cu pad. During the bonding operation, the all the Sn is transformed in Cu-Sn intermetallic compounds, resulting in a temperature stable bond. Such connections can also be realized without melting the Sn layer, resulting in a low bonding temperature. In addition, a no-flow underfill can be effectively used to realize reliable fine pitch micro bump interconnects. An example of such fine pitch Cu/Sn microbump interconnects is shown in figure 4.

For interconnect pitches of 10µm or below, the use of a Cu/Sn approach is more challenging. Direct Cu/Cu thermo compression bonding was used to bond 3D-SIC Cu TSV's directly to Cu bond pads using a hybrid collective bonding approach, shown in figure 3.[9]

6. Conclusions

3D interconnect technology follows the interconnect wiring hierarchy. Different technologies will address different types of 3D-integration at different levels of the interconnect hierarchy. 3D System integration by through-Si-via,TSV, technologies require the processing of three process modules: the TSV's, wafer thinning & thin wafer handling and the 3D stacking and packaging technology.

For coarse-pitch, large size, 3D-WLP post processed. TSV structures, a conformal Cu coating is to be recommended. For smaller 3D-WLP vias, 20 to 30 µm diameter, fully filled Cu vias can be effectively realized, provided the wafer thickness is reduced to about 50 µm.

3D stacked Integrated Circuits, 3D-SIC, with copper TSV first approach have been demonstrated with TSV diameters of 5µm and a pitch down to 10µm. Stacking 3D-SIC die at fine pitch is achieved using Cu/Cu thermo-compression approach.

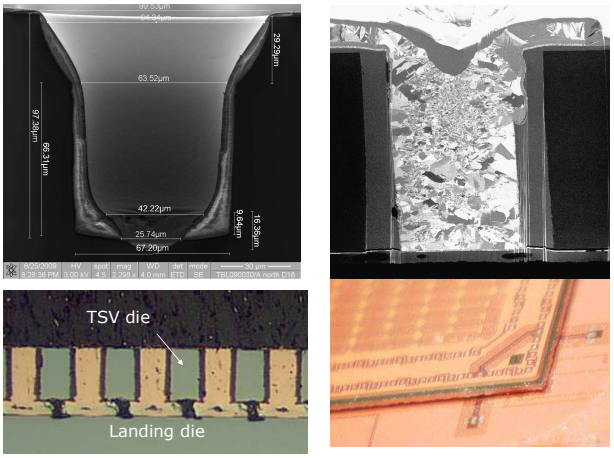

Figure 1: 3D-WLP TSV's. Top left: low AR, conformal Cu-TSV (photo-patterned, spin coated polymer liner) after Seed deposition, before plating; Top right: AR 2:1 filled TSV with annular polymer liner. Bottom: 3D-WLP TSV's with microbump on TSV, bonded to a landing die.

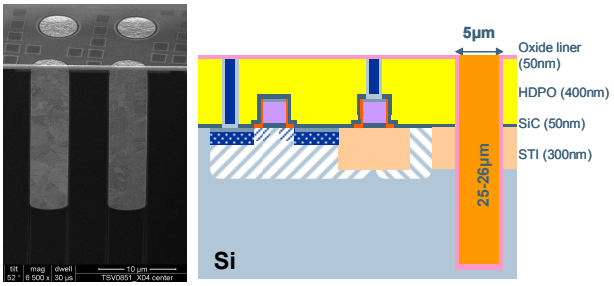

Figure 2: 3D-SIC TSV's realized after FEOL processing, before BEOL interconnect.

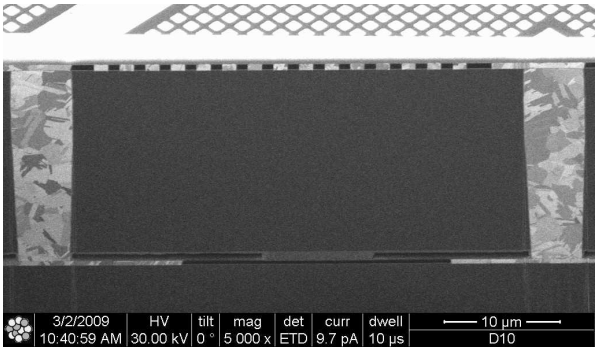

Figure 3: FIB of a Cu/Cu hybrid bonded 3D-SIC TSV die.

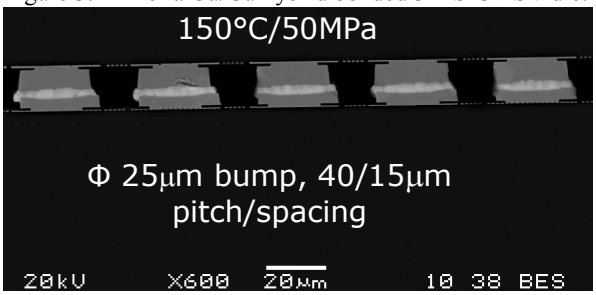

Figure 4: Cross-section face-to-face bonded die using 40µm pitch Cu/Sn micro bumps and no-flow underfill by diffusion reaction of Cu and Sn at low temperature (150°C)

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