Development of EEB (Electroplated-Evaporation Bumping) Technology for Fine Pitch and Low Resistance Cu/Sn Micro-Bumps

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1. Introduction
Three-dimensional (3-D) integration has attracted much attention because vertical stacked chips can increase packing density and improve chip performance. As packaging size is scaling down continuously with increasing demands for high I/O density, fine pitch micro-bumps are highly required to achieve miniaturized 3-D LSIs. We have proposed 3-D super chip consisting of microprocessor, memory, logic, and sensors. In order to realize 3-D super chip with high I/O, it would be required very fine pitch and low resistance micro-bumps. Solder and Cu electroplated bumps with pitch of 60 to 120 µm are widely used to electrically connect for LSI packaging in industry. Micro-bumping technologies where bump pitch is less than 50 µm using electroplating method have explored extensively for realization of miniaturized 3-D integration.

In this study, we developed electroplated-evaporation bumping (EEB) technology, which is a combination of Cu electroplating and Sn evaporation for the formation of low resistance and fine pitch micro-bumps. We successfully fabricated 5 µm square size and 10 µm pitch Cu/Sn micro-bumps for the first time. We formed bonded daisy chain samples with fine pitch and high-density Cu/Sn micro-bumps by thermal compression bonding. Good I-V characteristics were measured from the daisy chains consisting of 1000 bumps with 10µm square size. Resistance of Cu/Sn bump showed very low value approximately 30 mΩ.

2. Fabrication of fine pitch Cu/Sn micro-bumps
Fig. 1 shows fabrication process of Cu/Sn micro-bumps. Firstly, metal wiring layer was patterned by BCl₃/Cl₂ dry etching. Via holes were formed through PECVD layer by dry etching. Ta and Cu layers were deposited by sputtering methods as barrier and seed layers, respectively. Normally electroplating methods were used to form Cu and Sn bumps. However, they have difficulty to make uniform height bumps varied with bump size and density. Evaporation methods are candidates to make uniform metal layers. But, they have limitation to form thicker bumps. In this work, we developed EEB technology, which is a combination of Cu electroplating and Sn evaporation for the formation of low resistance and fine pitch micro-bumps. Resist of 10 µm thickness was patterned for the formation of micro-bumps. Cu bumps of 3 µm thick were quickly formed by electroplating and pure Sn layer of 2 µm thick was uniformly deposited on the wafer surface and onto Cu bumps by evaporation, sequentially. The wafer was dipped into acetone to lift off the resist except for via holes. Cu/Sn micro-bumps were formed on metal wirings only. Normally, wet etching method was used to remove Cu seed layer in industry. However, it has difficulty to form fine bump pitch less than 10 µm due to an undercut phenomenon during wet etching. In order to overcome undercut issue, we proposed Ar plasma sputtering method. Cu seed layer was clearly removed without undercut and damages by optimized plasma power and chamber pressure. Ta barrier layer was etched by CF₄ dry etching, sequentially. Cu/Sn micro-bumps with 5 µm square and 10 µm pitch were successfully formed for the first time as shown in Fig. 2. As seen from images, undercut phenomenon did not shown in under bump metallurgy (UBM) area. Average bump height is 5.0 µm and height variation is approximately ±3% (95%, 2σ) on the wafer level as shown in Fig. 3. Uniform bump height is very important to confirm a stable joining between high-density micro-bumps.

3. Evaluation of micro-joining characteristics
We fabricated daisy chain chips to evaluate micro-joining characteristics of fine pitch Cu/Sn micro-bumps. Fig. 4 shows a photograph of daisy chain chip consisting of 5 µm, 10 µm and 20 µm square bumps, respectively. The chip size was 5 mm × 4 mm. Two chips with high-density Cu/Sn micro-bumps were bonded by thermo compression bonding at 280 °C/1 min, 20 N and atmosphere environment without fluxing. Fig. 5 shows SEM image of the bonded Cu/Sn bumps with 10 µm square size. Alignment accuracy was approximately 3 µm. Good I-V characteristics were measured from the daisy chains consisting of 1000 bumps with 10 µm square size. Resistance of Cu/Sn bump showed very low value approximately 30 mΩ. We proposed unique micro-bumping technology, EEB and the dry etching methods to remove seed/barrier layers for
fine pitch and low resistance Cu/Sn bump. We succeeded to form 10 µm pitch Cu/Sn bump for the first time. It shows uniform bump height. Good I-V characteristics were measured from the daisy chains consisting of 1000 bumps with 10 µm square size. Resistance of bump is very low approximately 30 mΩ. From these results, we confirm EEB technology could be an attractive solution for 3-D super chip integration.

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References