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High-Aspect-Ratio Fine Cu Sidewall Interconnection over Chip Edge with Tapered Polymer for MEMS-LSI Multi-Chip Module

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1. Introduction

Recently, heterogeneous system integration involving CMOS, MEMS, optics, and biochips has attracted much attention due to its high functionality, potential applications and low power consumption. Fig. 1(a) shows a conceptual structure of hetero-integrated MEMS-LSI multi-chip module we have proposed. In order to realize the multi-chip module, we developed several key technologies such as multi-chip fluidic self-assembly, high-density micro bump formation, and passive devices on a chip as shown in Fig. 1(b) [1].

In this work, we proposed unique Cu sidewall interconnection crossing-over chip edge with large step height for realizing heterogeneous MEMS-LSI multi-chip module. Cu sidewall interconnection has several advantages comparing with conventional wire bonding interconnection. Enormous interconnections can be simultaneously formed on the MEMS-LSI module. Fine width sidewall interconnection less than 10um can be formed for high density integration. Sidewall interconnection has relatively short length compared with bonding wire in which it can be reduced RC delay of interconnection for high performance integration. However, it is not easy to make sidewall interconnections directly crossing-over chip edge with large step coverage by conventional LSI processes. We developed high aspect ratio Cu sidewall interconnection crossing-over chip edge with large step coverage by optimizing photolithography and electroplating methods and by applying tapered polymer structure at sidewall of the chip. Cu sidewall interconnections of 10μm width were successfully formed crossing-over the chip edge with large step height of 100μm. Good fundamental functions of LSI chips connected through Cu sidewall interconnections were obtained in the test module.

2. Fabrication of Cu Sidewall Interconnections

Fig. 2 shows the fabrication process of Cu sidewall interconnections. At first, contact holes were formed on chips and substrate by dry etching methods, respectively. Barrier layer of Ti and seed layer of Cu were deposited using RF sputtering. A thick photoresist(PR) was spin coated and patterned. Cu sidewall interconnections were formed by electroplating method. Ti and Cu layer were removed by wet-etching methods. However, there is a big technical challenge to make Cu sidewall interconnection. As LSI chips have large step height above 100μm, it is hard to cover over chips with conventional low-viscosity PR. High-viscosity PR is prefer to cover large step height. However, PR was accumulated very thickly at sidewall of the chip, and it is very difficult to pattern fine and uniform interconnections through thick PR. Fig. 3 shows SEM images of Cu sidewall interconnection (Design Rule, 10μm) fabricated under not-optimized conditions. Non-uniform and larger width sidewall interconnections were formed as shown in fig. 3(a) and Cu sidewall interconnections were disconnected at the bottom area as shown in fig. 3(b). To overcome these problems, we optimized the spin coating process of thick PR and the exposure conditions. Uniform Cu sidewall interconnections of 20μm width were fabricated crossing-over the chip edge with large step height of 100μm as shown in Fig. 4. However, the width is still larger than the design rule of 10μm. It has limitation to scale-down the width of sidewall interconnection only changing the exposure conditions. In order to narrow the width of interconnection, we proposed the tapered polymer structure at sidewall of the chip as shown in Fig. 5. Tapered polyimide structure can be reduced the resist thickness at the chip sidewall and it would be decreased the exposure doze. Therefore, it can be assist to make fine patterns. We optimized the tapered shape and slope of polymer. Fig. 6 shows Cu sidewall interconnection with the tapered polyimide structure. As clearly seen from the images, uniform and fine Cu sidewall interconnections with 10μm width were successfully realized crossing-over the chip edge with 100μm height.

3. Evaluation of Cu Sidewall Interconnections

We evaluated electrical characteristics of fine Cu sidewall interconnections as shown in Fig. 7. Resistances of Cu sidewall interconnections show relatively small distributions. Average electrical resistivity is 1.65×10^{-6}(Ω cm), which is close to calculated value. High topography step was having only a small influence on the lateral coverage of Cu interconnections. We fabricated the test module containing LSI chips with 100μm height, which were electrically connected by Cu sidewall interconnections as shown in Fig. 8. Good fundamental functions of the LSI chips on the module were obtained through Cu sidewall interconnections crossing-over them as shown in Fig. 9.

4. Conclusion

High-aspect-ratio fine Cu sidewall interconnection has developed. We succeed to form uniform and fine Cu sidewall interconnection with 10μm width crossed-over the chip edge with 100μm height by applying the tapered polyimide structure and optimizing exposure conditions.
Cu sidewall interconnections have good electrical characteristics. The results of the test module measurement confirmed that this is a reliable process for interconnecting the heterogeneous MEMS-LSI multi-chip module.

Acknowledgement
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References

[1]T. Fukushima et al., IEDM Tech. Dig., pp. 499-502 (2008).

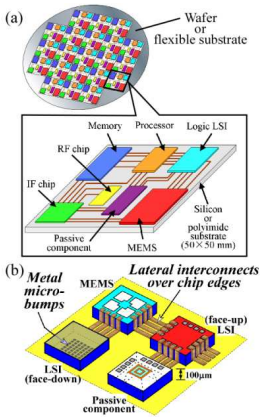


Fig.1 (a) Conceptual structure of hetero-integrated MEMS-LSI multi-chip module (b) Key technologies for multi-chip module

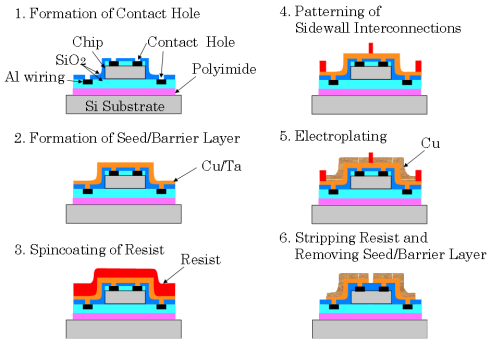
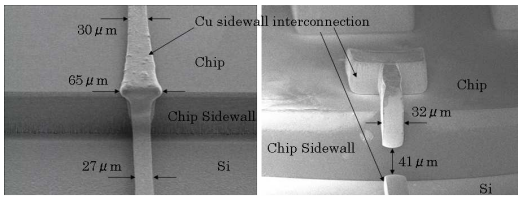
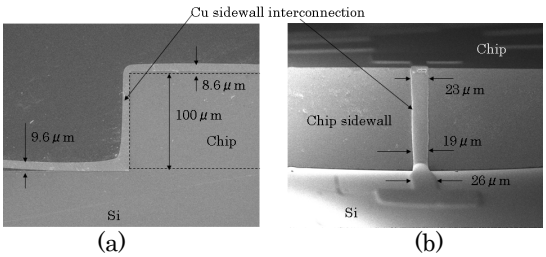


Fig.2 Fabrication process of Cu sidewall interconnections



(a) (b)

Fig.3 Cu sidewall interconnections which were fabricated under non-optimized conditions



(a) (b)

Fig.4 (a) Cross sectional SEM image and (b) planer SEM image of Cu sidewall interconnection

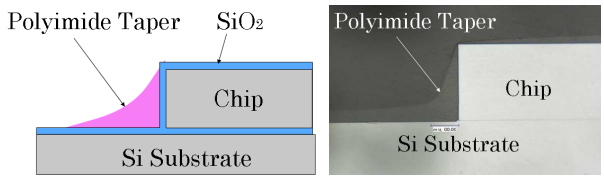
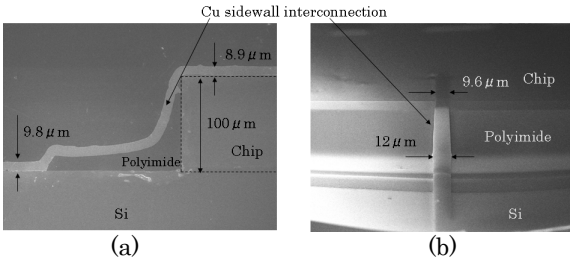


Fig.5 Concept of the tapered polyimide structure



(a) (b)

Fig.6 (a) Cross sectional SEM image and (b) planer SEM image of Cu sidewall interconnection with the tapered polyimide structure

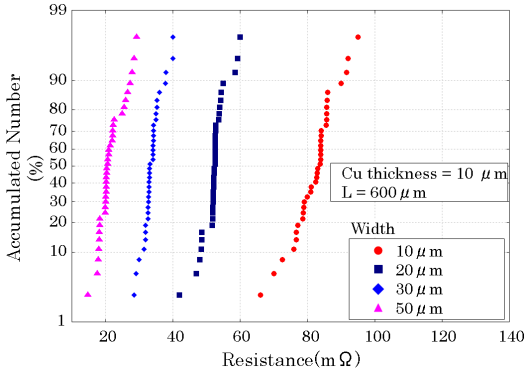
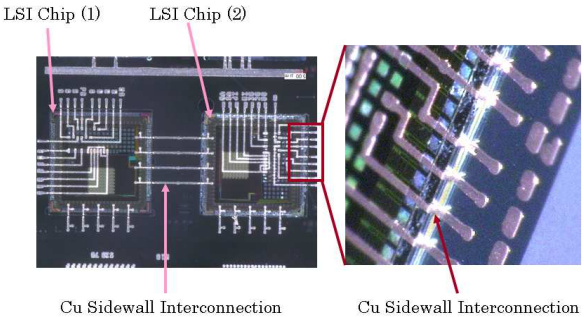


Fig.7 Resistance of Cu sidewall interconnections



(a) (b)

Fig.8 Optical microscopic images of (a) the test module and (b) Cu sidewall interconnections on the test module

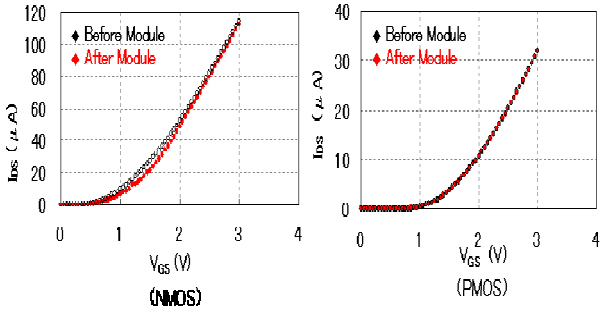


Fig.9 I_d-V_g characteristics of LSI circuits connected through Cu sidewall interconnections on the module