# **Back-Side Illuminated CMOS Image Sensor Fabricated Using Compliant Bump**

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## 1. Introduction

Three-dimensional (3D) chip stacking technology is attracting considerable attention for realizing advanced, highspeed, compact, and highly functional electronic systems [1-3]. 3D systems, particularly, systems containing an array of circuit elements such as image sensors, require reliable highdensity inter-chip connections. In order to meet the requirements of 3D systems, we have proposed compliant bumps [4,5] such as Au pyramid bumps and Au cone bumps.

Since these bumps can be easily deformed under compression, we expect the following effects: (1) reliable bonding at low temperature, (2) reducing strain generation at the device level, (3) suppression of bonding failure, and (4) resin exclusion for chip stacking with a precoated-resin. In the previous study [4-8], we confirmed the above effects [4-6] and stacked very-thin chip (thickness = about 20  $\mu$ m) having 30,600 interchip connections using the compliant bumps [7].

In this study, using the compliant bump technology, we demonstrate the fabrication of back-side illuminated CMOS image sensor by stacking a very-thin back-side illuminated photodiode array chip onto a CMOS read-out circuit chip.

#### 2. Fabrication process

Figure 1 shows the fabrication process of the back-side illuminated CMOS image sensor. The n+/p photodiode array wafer and the CMOS read-out circuit wafer were fabricated by using a standard 0.35  $\mu$ m CMOS process. A low-stress wafer handling system was applied to thinning of the photodiode array wafer down to 21  $\mu$ m-thick, the formation of TSV (1 array between the formation of TSV) TSV (through silicon via), and the back-side electrode on a very-thin photodiode array wafer. First, Au cone bumps were formed on the photodiode array wafer (Fig. 1(a)). Then, the support glass with through-holes was bonded to the photodiode array wafer by an adhesive. The photodiode array wafer was thinned by grinding and dry polishing (Fig. 1(b)). Cu TSVs were then formed by deep Si etching by a non-Bosch technique, deposition of a conformal TEOS CVD, selective removal of the insulator at the bottom of the via, deposition of a conformal barrier-seed metal (Ta-Cu) layer, Cu electroplating, and Cu/Ta CMP (Fig. 1(c)). For the interconnection to the p-type region of the n+/p photodiode and optical shadowing, Al back-side electrodes were fabricated (Fig. 1(d)). After bonding the support tape to the back-side of photodiode array wafer, which prevents the very-thin wafer from cracking during dicing, the support glass was separated from the photodiode array wafer by injecting the solvent into the adhesive from the through-holes of the support glass (Fig. 1(e)). Then, the photodiode array wafer and the CMOS read-out circuit wafer were diced. After the support tape was separated by heating, the very-thin photodiode array chip and the CMOS read-out circuit chip were bonded (Fig. 1(f)). Bonding conditions were as follows: pressing load, 9 kgf (0.53 gf/bump); bonding temperature, 300°C; and bonding time, 20 s.

## 3. Characteristic

Figure 2 shows a cross sectional SEM image of the image sensor comprising very-thin back-side illuminated photodiode

array chip stacked on the CMOS read-out circuit chip. We observe that a very-thin photodiode array chip with a thickness of 21  $\mu$ m is connected to the CMOS read-out circuit chip through the cone bumps.

Figure 3 shows the characteristics of the photodiode. We find that the photodiode characteristics remained unchanged after chip stacking. This result suggests that compliant bump reduces strain generated at the photodiode. We also find that light current maximizes at wavelength of 700 - 900 nm.

Figure 4 shows the test circuit board prepared for evaluating the image sensor. Dynamic images obtained by the image sensor were sent to a PDA through an RF transmit module (Bluetooth). Some examples of image flames ( $128 \times 128$  pixels) are shown in Fig. 5. We observe no defects in these image flames.

In addition to the results described, we have succeeded in bonding bump array whose number is as large as VGA(Video Graphic Array,  $640 \times 480$ ) class pixels [8].

These results demonstrate the effectiveness of the compliant bump technology for creating a new imaging device.

## 4. Conclusion

Using a compliant bump technology, we demonstrated the fabrication of back-side illuminated CMOS image sensor comprising very-thin back-side illuminated photodiode array chip and CMOS read-out circuit chip. The integration process of TSV, back-side metallization, dicing, and chip bonding of a very-thin wafer down to a 21  $\mu$ m thickness has been developed using the novel glass support in conjunction with a polymer support process. The results demonstrate that the compliant bump technology is very effective in creating 3D systems such as new imaging device.

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#### (a) Fabrication of Au cone bump



(b) Bonding of support glass, Wafer thinning



(c) Formation of TSV (Through-Silicon Via)



(d) Formation of back-side electrode



(e) Bonding of support tape, Separation of support glass



(f) Dicing, Separation of support tape,

Bonding to CMOS read-out circuit chip



**Fig. 1:** Fabrication process of back-side illuminated CMOS image sensor fabricated by using the compliant bump technology.



Fig. 2: SEM image of the back-side illuminated CMOS image sensor. Thickness of photodiode array chip is 21  $\mu$ m. Bump pitch is 24  $\mu$ m.



**Fig. 3:** Characteristics of photodiode: (a) Dark current before and after chip stacking. (b) Light current under back-side illumination. Photodiode characteristics remained unchanged after chip stacking.



**Fig. 4:** Print circuit board prepared for evaluation of the image sensor. Dynamic images taken by the image sensor are transmitted to a PDA using an RF transmitter.



Fig. 5: Examples of image flames ( $128 \times 128$  pixels).