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System-on-Package Platform with Decoupling Capacitor Integration and Thermal Performance Improvement

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1. Introduction

Integration of a decoupling capacitor is important to realize a fully integrated system-on-package (SOP) in which capacitance of 1-100 nF is required for the decoupling [1]. Even with a high-k dielectric, it is hard to get capacitance density larger than 5 nF/mm^2 with planar capacitors [2]. For higher capacitance density, three-dimensional (3D) capacitors can be an alternative solution. Integrated 3D capacitors were investigated by several groups [2]-[5].

Recently, a system-in-package concept for integration of 3D capacitors and active chips by flip-chip interconnection using solder bumps has been published [6]. However, due to the limitation of diameter and pitch of solder bumps, distance between flip-chip bumps should be large enough to be electrically separated. This causes the degradation of the electrical [7] and thermal performance of the active chips which are important issues in packaging. Flip-chip bonding on the ohmic contacts of an active chip can improve the thermal performance by reducing the distance from the junction to the heat sink. It is possible to make this bonding structure by Si bumps because of its capability of making fine patterns with high aspect ratio.

Flip-chip bonding using Si bumps showed improved thermal performance in the SOP technology [8]. However, flip-chip bumps were only located on the gate, source, and drain pads of an active chip. To further improve thermal performance, flip-chip bumps should be located near the junction.

In this paper, an SOP technology on high resistivity silicon (HRS) substrate with decoupling capacitor integration and thermal enhancement by novel flip-chip bonding is described. The details of the proposed SOP technology are analyzed in the following.

2. Fabrication of an SOP platform

The concept of the SOP technology with decoupling capacitor integration and thermal performance improvement is shown in Fig. 1. A distinctive feature of the proposed structure is the Si trenches and bumps which are patterned simultaneously. To fabricate the Si trenches and bumps, a 5000 Å SiO_2 was deposited on a substrate and patterned as an etch mask. The substrate was dry-etched with the Bosch process until a depth of 30 μm was achieved. Si trenches had a pitch of 5 μm and an aspect ratio of about 7. After Si trenches and bumps were defined, thermally grown 1000 Å SiO_2 was deposited to smooth the etched Si surface. 3D capacitors were fabricated on the surface of the trenches. Other passive devices such as thin-film resistors (TFR), inductors and filters were fabricated on the substrate as well. Backside of the substrate was thinned as 250 μm to reduce the thermal resistance from the junction to the heat sink. Finally, Au/Sn bumps were electroplated on Si bumps for flip-chip bonding of a GaAs chip.

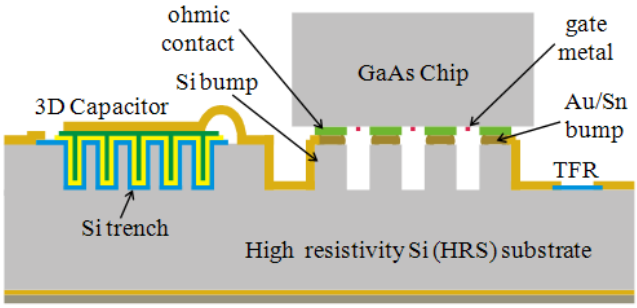


Fig. 1. Structure of the proposed SOP platform.

3. 3D Capacitor for decoupling

N^+ polycrystalline silicon (poly-Si) was adopted as the electrodes. In spite of the low conductivity of a poly-Si compared with other metals, it was chosen as the electrodes owing to its good step coverage when deposited by LPCVD. To address the conductivity problem, we introduced the $POCl_3$ doping [3] to the poly-Si and even modified the doping process to obtain the highest conductivity as possible. As a result, the highest conductivity of 2×10^5 S/m, equivalent to the sheet resistance of 7 Ω/square was achieved for the n^+ poly-Si. After bottom electrode of 7000 Å poly-Si was formed, 300 Å SiN_x was deposited by LPCVD at 800 °C as a capacitor dielectric. Top electrode of a 5000 Å poly-Si was formed using the same process as the bottom electrode. Next, pads of the 3D capacitor were electroplated with 4 μm Au. Figure 2 shows the picture and the SEM image of the fabricated 3D capacitors.

The extracted intrinsic capacitance density and capacitance over varying capacitor area are plotted in Fig. 3. The achieved capacitance density and the capacitance were 22 nF/mm^2 and 4-61 nF, respectively. The 3D capacitors exhibit 10 times higher capacitance density compared with planar capacitors, due to the increased effective capacitor area formed by the Si trenches. Extracted equivalent series inductance (ESL) was in the range of 64-92 pH. It shows that the fabricated 3D capacitors are suitable for the high speed decoupling.

4. Novel flip-chip bonding for thermal enhancement

Thermal performance should be considered in the

package. The heat generation occurs in the vicinity of the channel. GaAs which is a popular material in compound semiconductor has low thermal conductivity (46 W/mK). Thus, thermal resistance through the GaAs substrate is relatively high. We proposed a novel flip-chip bonding structure using Si bumps to reduce the thermal crowding around the channel. In the proposed structure, Si bumps are directly attached on the ohmic contacts of the GaAs chip, thus thermal resistance from the junction to the heat sink are lowered effectively. To avoid the electrical connection and RF loss through the substrate, HRS was used as the substrate.

3D finite element method thermal simulations were executed to verify the proposed structure. A GaAs HEMT which has 10 gate fingers with 35 μm pitch, and 100 μm width was used in the simulation. The output power density of the GaAs HEMT was set up as 1 W/mm. The simulation structure is depicted in Fig. 1. Ideal heat sink of 25 °C is located under the HRS substrate. In the flip-chip bonding structure, heat flows through Au/Sn bumps and Si bumps which have 20 μm width. Table. 1 shows the thermal conductance and the thickness of each layer used in the simulation. For a comparison with a flip-chip bonding structure, a GaAs HEMT of 100 μm thickness without flip-chip bonding was also simulated.

Figure 4 shows the simulation results on both structures. The peak temperature of the device by using flip-chip bonding was reduced by 38 % from 122 °C to 76 °C. Besides, it is shown in Fig. 4 that thermal crowding around the channel was definitely reduced. This is because of i) the high thermal conductivity of the Si bumps, and ii) the location of the flip-chip bumps near the junction. Also thanks to Si bumps, bonding of a chip with fine gate pitch is possible. To verify the simulation results, a GaAs chip was flip-chip bonded on the proposed SOP platform and the electrical measurement is ongoing.

5. Conclusion

Novel Si-based SOP structure was proposed. Integrated 3D capacitors using Si trenches had capacitance density of 22 nF/mm^2. These 3D capacitors can be used as decoupling capacitor in high speed application due to its low ESL compared with conventional chip capacitors. Thermal simulation showed a flip-chip bonding on the ohmic contacts of GaAs HEMT using Si bumps is effective to reduce the thermal resistance from the junction to the heat sink. Due to the high aspect ratio of Si bumps, it can be applicable to the flip-chip bonding of a microwave chip.

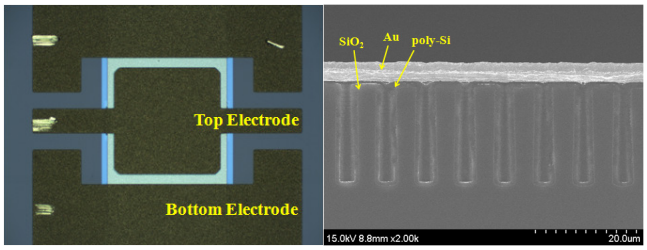


Fig. 2. Photograph and SEM image of the 3D capacitor.

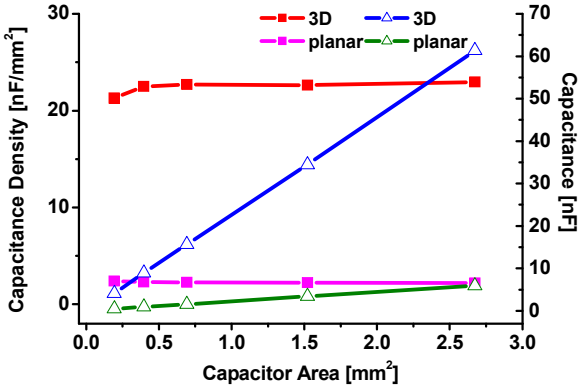
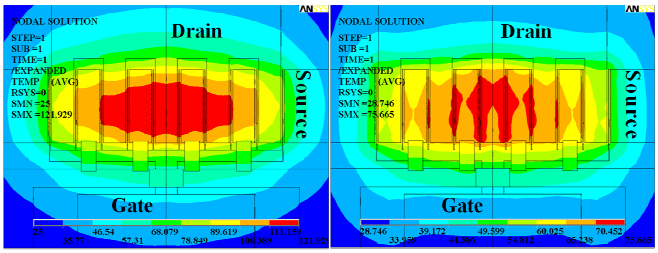


Fig. 3. Measured capacitance density, capacitance 3D capacitor vs. planar capacitor (■: Capacitance density, △: Capacitance).

Layer	Thermal conductance (W/mK)	Thickness (μm)
GaAs substrate	46@300K	100, 625
Au/Sn bump	57	3
Si bump	149@300K	30
Si substrate	149@300K	220
Die adhesive	29	10

Table. 1. Thermal conductance and thickness of layer materials used in thermal simulation.



(a) Without flip-chip bonding. (b) With flip-chip bonding.

Fig. 4. Thermal simulation results of the GaAs HEMT.

Acknowledgement

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