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Stabilities of La_2O_3 Metal-Insulator-Metal Capacitors Under Constant Voltage Stress

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1. Introduction

Recently, high-k metal-insulator-metal (MIM) capacitors integrated into backend interconnection as passive components have generated great interest for analog and RF applications [1], [2]. The stability of MIM capacitors is a key issue on precision performance, especially on the voltage linearity. Some studies [3], [4] have discussed the capacitance variation of SiO_2 MIM capacitors during electrical stress. However, the degradation of the MIM capacitor with high-k dielectric has not been well characterized. In this paper, the behaviors of La_2O_3 MIM capacitors under constant voltage stress (CVS) were investigated. The correlations among the injected charges (Q_{inj}), the capacitance change ($\Delta C/C_0$), the quadratic voltage coefficient of capacitance (α), and the dielectric loss (D) of the La_2O_3 MIM capacitor were also discussed.

2. Device Fabrication and Experimental Procedures

This work focused on a 10-nm La_2O_3 MIM structure with an 11.4-fF/μm^2 capacitance density and an area of 2500 μm^2. The schematic layout and the schematic cross section of the capacitor along the A-A' line in the layout are shown in Figs. 1(a) and 1(b). The high-k dielectric La_2O_3 film was deposited by e-beam evaporation and annealed in O_2 ambient to improve its quality. The top bi-layer (TaN/Ni) and bottom (TaN/Ta) electrodes were deposited by a reactive sputtering. All process temperatures during MIM capacitors fabrication were below 400 °C compatible with backend process. The samples were subjected to constant voltage stress in the range of –4.2 V to –5 V applied on the top electrode (Ni), and their capacitances variation were also measured at 25°C using an LCR meter at various intervals during CVS testing.

3. Results and Discussion

Fig. 2 shows *C-V* and *J-V* characteristics of the 10-nm La_2O_3 MIM capacitor. The leakage current is below 10^{-7} A/cm^2 under the applied voltage of ±2 V. The quadratic voltage coefficient (α) of capacitance could be fitted by the second order polynomial equation: $C(V) = C_0 \cdot (\alpha \cdot V^2 + \beta \cdot V + 1)$, where C_0 is the capacitance at zero bias. Hence, the values α of 10-nm La_2O_3 MIM capacitor measured at 10 kHz and 100 kHz are 775 ppm/V^2 and 671 ppm/V^2, respectively.

Fig. 3 illustrates the correlations among the relative capacitance variation $[C_0(t)-C_0(0)]/C_0(0)$, the stress time, and the injection charges (Q_{inj}) at various CVS voltages from –4.6 V to –5 V, where $C_0(t=0)$ is an initial capacitance at zero bias. As shown in the inset of Fig. 3, the relative-capacitance variation increases with a logarithmic increase in Q_{inj} regardless of the stress biases, which implies charge trapping in dielectric films [5]. When the carriers inject into the La_2O_3 dielectric film during CVS stress, the trapped charges could generate dipoles to increase the local permittivity and then contribute to the degradation of the capacitance [3], [4]. Besides, as shown in Fig. 3, after the $[C_0(t)-C_0(0)]/C_0(0)$ rapidly increases in the initial stress, it tends to saturate after the 1000-s stressing. This saturation could be attributed to the trapped charges near the top electrodes. After the pre-existing trap states are rapidly filled by injection charges to increase the capacitance, the trapped charges would increase the barrier height near the injection electrode and result in a saturation phenomenon [6].

Fig. 4 depicts the 10-year stability extraction of a fabricated 10-nm La_2O_3 MIM capacitor estimated by the relative-capacitance variation. It could be obtained from the extrapolated $[C_0(t)-C_0(0)]/C_0(0)$ versus stress time to 10 years, as shown in the inset in Fig. 4. The 10-year degradations of 10-nm La_2O_3 MIM capacitors with an 11.4-fF/μm^2 capacitance are 6.32 %, 4.09 %, and 2.61 % under –4.6 V, –4.4 V, and –4.2 V, respectively. The safety 10-year operation voltage with below 1-% degradation could be extrapolated by around –4 V. This long-term stability is useful for the sub-65 nm technology node, whose operating voltage is smaller than 1.5 V.

Time dependence of $\alpha(t)$ normalized to its initial value $\alpha(0)$ under CVS biases from –4.6 V to –5 V is plotted in Fig. 5. The inset presents the dependence of $\alpha(t)/\alpha(0)$ on the relative variation in dielectric loss $[D_0(t)-D_0(0)]/D_0(0)$ during stressing, where $D_0(0)$ is the fresh dielectric loss at zero bias. It can be found that $\alpha(t)/\alpha(0)$ decreases with the increasing stress time for a certain stress bias. The reason for the decrease in the voltage dependence of capacitance is that the carrier mobility is reduced by the stress-induced trap states, and then hardly follows the alternating signal with a higher relaxation time [7]. Besides, $\alpha(t)/\alpha(0)$ linearly decreases with a logarithmic increase in relative dielectric loss, but it still maintains almost the same slope under various stress voltages. It further verifies the change in voltage dispersion of capacitance is ascribed to the stress induced traps.

Dependence of $\alpha(t)/\alpha(0)$ on stress time under a CVS of –4.8V with various measurement frequencies is exhibited in Fig. 6, and the inset presents the dependence of $\alpha(t)/\alpha(0)$ on the relative variation in dielectric loss $[D_0(t)-D_0(0)]/D_0(0)$. As the measurement frequency increases, the changes in $\alpha(t)/\alpha(0)$ become smaller, and the correlation between $\alpha(t)/\alpha(0)$ and the relative variation in D has been confirmed again.

4. Conclusions

The stabilities of MIM capacitors with La_2O_3 dielectric under CVS are investigated in this paper. It could be found that the degradation in capacitance is dependent on injected charges (Q_{inj}). The correlation between the carrier injection and the relative-capacitance variation of La_2O_3 MIM capacitors is also evaluated. The improvement in voltage nonlinearity of La_2O_3 MIM capacitors during CVS testing could be attributed to the stress induced traps in dielectrics. Additionally, highly stability of 10-year lifetime was achieved for a 10-nm La_2O_3 MIM capacitor with an 11.4-fF/μm^2 capacitance density.

References

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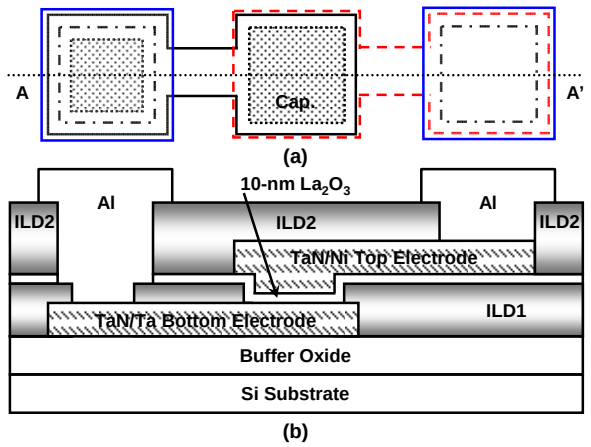

Fig. 1. The schematic layout of the La_2O_3 MIM capacitor. (b) The schematic cross section of the capacitor along the A-A' line in the layout shown in (a).

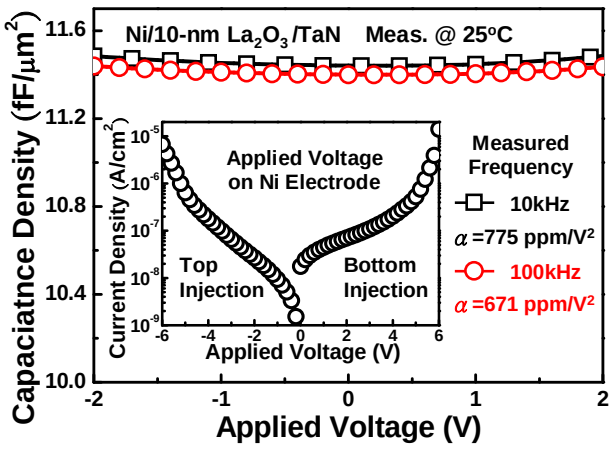

Fig. 2. The *C-V* curve, *J-V* curve, and the quadratic voltage coefficient (α) of a typical 10-nm La_2O_3 MIM capacitor.

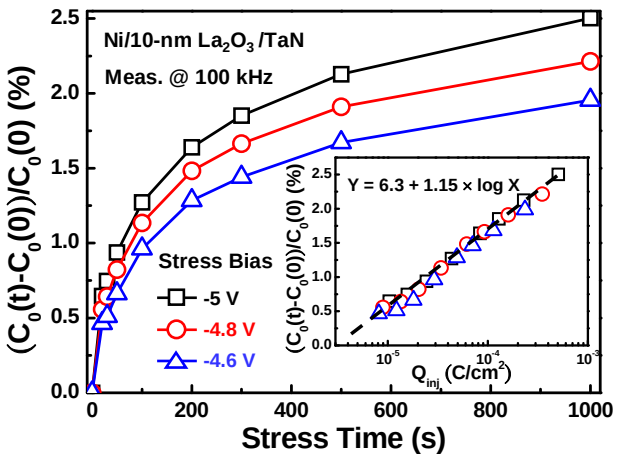

Fig. 3. Relative-capacitance variation $[C_0(t)-C_0(0)]/C_0(0)$ as a function of stress time and injection charges (Q_{inj}) at various CVS voltages from –4.6 V to –5 V.

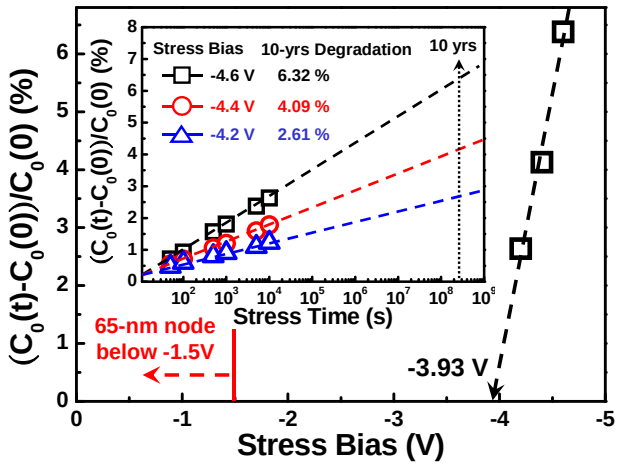

Fig. 4. The 10-year stability extraction of 10-nm La_2O_3 MIM capacitors estimated by the relative-capacitance variation.

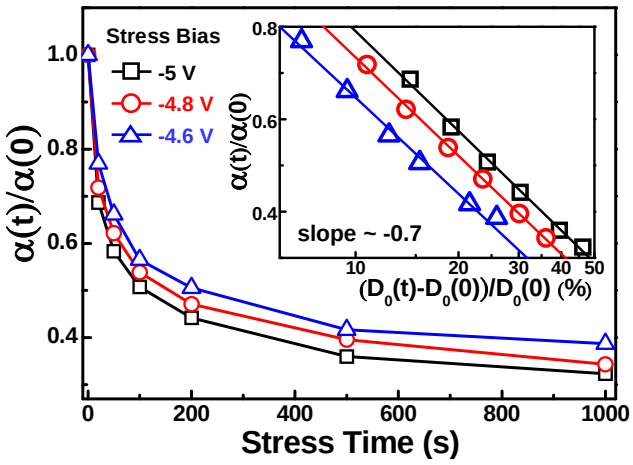

Fig. 5. Time dependence of the relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(0)$ under a CVS of –4.6 V to –5 V.

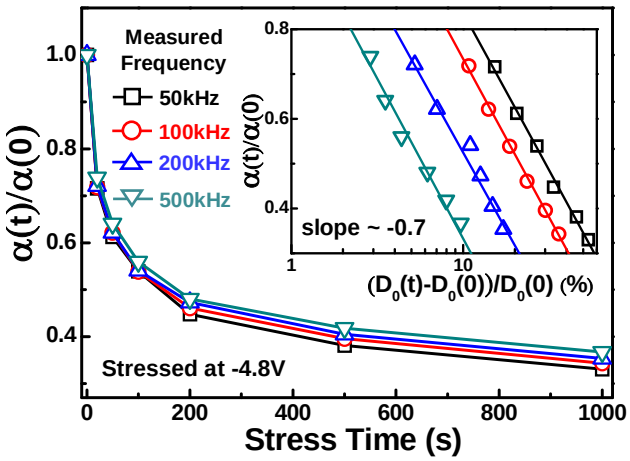

Fig. 6. Time dependence of the relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(0)$ under a CVS voltage of –4.8 V with various measurement frequencies.