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Patterning & metallization options for advanced contact module integration

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Abstract

In this paper the main challenges associated to scaling the contact module are discussed. Bother patterning and metallization aspects are addressed.

Patterning

Contact diameter/pitch scaling requirements for DRAM and MPU are summarized in Table 1. Immersion lithography with NA=1.35 can theoretically fulfill these until the 2011-2012 timeframe, but only through design split and use of innovative double exposure [2] or double patterning schemes [3] or ultimately a combination of both. An example of a double exposure technique relying on use negative tone resist which can deliver ~40nm contacts at 80nm pitch with excellent uniformity is shown in Fig. 1. Implementation of these techniques is obviously more straightforward for regular contact designs, typical to memory, as compared to logic since for the latter through pitch solutions are required. EUV lithography can deliver the aggressive pitch resolution scaling well beyond the earlier indicated timeframe in a single exposure without need for proximity corrections on the mask. However further development on the power delivered by the source, on increasing throughput and on dedicated EUV mask and resist technology is required before this next generation litho can be considered mature for production [4].

Both double patterning techniques and the limited resist thickness used in EUV call for the introduction of either trilayer resists or hard mask. Both metal and amorphous carbon based hard masks have been integrated into electrically functional SRAM contacts (Fig. 2) [5]. While the metal hard mask is removed in the CMP step, the amorphous carbon layer is stripped at the end of the contact patterning sequence, making it more compatible with subsequent sputter based pre-metallization cleans.

To ensure good contact to gate-overlay on tight gate pitches a further downscaling of the contact diameter might be required. Besides solutions relying on shrinking the dimension of the feature in the printed resist or on sloped contact etch processes, a plasma assisted shrink step can be introduced as part of the etch sequence [6]. In Fig. 3, an example of this is shown where 90nm printed contacts are reduced down to 43nm. However, upon applying aggressive shrink, careful process tuning is required in order to achieve good pattern fidelity on large features, such as alignment marks, required for integration subsequent mask levels [7].

Both post etch/ash wet clean and the clean prior to metal barrier deposition have been shown to require optimization to avoid queue time effects [8]. The latter clean process needs to be carefully tuned towards integration on scaled junctions/silicide to avoid silicide punch through, potentially resulting into increased junction leakage. Self-limiting and selective chemical dry cleans induce the least recess into the silicide and can deliver slightly lower contact resistance and improved uniformity [9], but may be vulnerable to a non-residue free patterning process (Fig. 4).

Metallization – Cu vs W

The mainstream route for metallization has been a W fill based module on Ti/TiN barrier since many technology nodes. For sub-50nm dimensions however, the conventional MOCVD based TiN barrier film will have to be replaced by a more conformal ALD film to enable void free filling down to at least ~30nm dimensions (Fig. 5). The lower contact resistance values and improved uniformity for the ALD film on sub-50nm dimensions (Fig. 6) is attributed to the smaller W keyhole size on plugs with ALD barrier. Plug resistance can also be influenced through tuning the W deposition itself towards a lower resistivity film by promoting growth of larger grains [10]. WN can be an attractive alternative to Ti/TiN as a cost-effective W barrier since it can be deposited on one and the same platform as the W fill material [11] but may be vulnerable to residual oxide left at the contact bottom for which the Ti base layer remains the most effective effective getter layer.

With the parasitic contribution of the plug resistance to the overall device resistance becoming increasingly important [12], there is growing interest in trying to postpone this effect by using Cu as fill material [13]. Besides anticipated small improvements to the transistor Ion/Ioff characteristics, cost related benefits of using Cu cannot be neglected, including re-use of the existing toolset for Cu damascene and the potential to process CA/M1 modules in dual damascene mode [14]. Conventional PVD deposited based TaN/Ta barrier and Cu seed technologies used in damascene BEOL integration are limited in terms of scaling contact diameter and AR. As a result, similar to the W module, ALD or CVD based barrier layers are under consideration. The capabilities of a bilayer barrier approach using PVD Ta(N)/ALD TaN have been demonstrated on relaxed dimensions in [15]. The scalability of this module towards sub-50nm contacts is demonstrated in Fig. 8, with contact resistance values remaining below 100Ω for the smallest contacts in the experiment. Possible alternative Cu contact barriers include ALD or CVD based Ru [16] or Co [17], each time deposited on a PVD Ta(N) base layer. These Ru and Co films may have the particular advantage of being able to serve as a Cu seed enhancement layer enabling Cu electroplating on very narrow features. Electrically functional Cu contacts on Ru have been reported recently on sub-30nm dimensions[16].

Reliability of Cu contacts

Whereas the role of the W barrier is limited to enabling void free filling, in case of Cu there is a potential risk for compromising device integrity. Screening the effectiveness of candidate Cu contact barrier can be done prior to integration through monitoring formation of Cu-silicide related XRD peaks upon annealing [18].

Elaborate studies on the reliability of the integrated Cu module under thermal and/or electrical stress have been reported on in [19,20]. These studies indicated that upon using optimized barrier conditions there is no indication for any front-end yield or reliability issue linked with the use of a Cu contact module. However, defective Cu barrier, specifically at the contact bottom by e.g. too aggressive resputter conditions on a PVD Ta(N) barrier, gives rise to either leaky junctions and/or broken gate oxides and reduced TDDB lifetimes (Fig. 9).

Alternatives to Cu & W

While W or Cu based contact fill have proven extendibility to at least 30nm dimensions, alternatives to W or Cu are being explored as well. Some report on alternative fill materials such as electroplated Rh, deposited on Ti/Ru [21], of which the intrinsic resistivity is situated between W and Cu. But this option is particularly challenged at CMP.

Self-aligned processes could sustain scaling further. An example of this is the all wet bottom-up electroless Ni-based fill proposed in [22]. Also contacts formed through (PE)-CVD based growth of carbon nanotubes (CNTs) fall into this category, having the additional advantage of their excellent current carrying capacity since contact current density is expected to rapidly increase as well. Many issues need to be overcome however, linked to the deposition of the catalyst in small features and the need to further increasing the CNT bundle density to outperform the conventional metal based fills in terms of contact resistance, as evaluated on relaxed dimensions [23,24].

Conclusions

In this paper we addressed the challenges faced by both patterning and metallization steps in view of scaling requirements for the contact module. Design splits will be required to sustain pitch scaling prior to the anticipated introduction of EUV technology. This will drive a need for hard mask based etching. Clean steps will need to further align to scaling trends on junction/silicide modules. W metallization is shown to be scalable down to ~30nm upon introducing ALD TiN barrier but even then resistance values rapidly surpass 100Ω on sub-50nm dimensions. The Cu module is shown to be a viable alternative to postpone the resistance increase, but also requires material or technology changes to the barrier/seed layers to enable further downscaling and to maintain long term device integrity.

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Table 1: Scaling of contact dimensions for memory and logic as predicted by the ITRS roadmap [1]

Item	'09	'10	'11	'12	'13	'14	'15
DRAM ½ pitch (nm)	50	45	40	36	32	28	25
Contact after etch (nm)	50	45	40	36	32	28	25
MPU M1 ½ pitch	52	45	40	36	32	28	25
Contact after etch (nm)	58	51	45	40	36	32	28

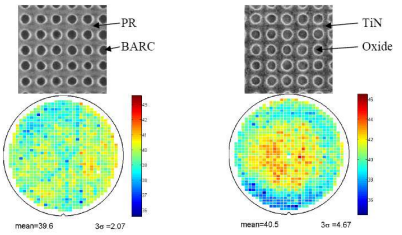

Fig. 1: CD uniformity at pitch 80nm after double exposure using the negative tone development technique, after litho (left) and after transfer into a TiN hard mask (right) [2].

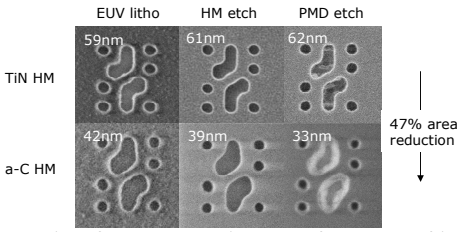

Fig. 2: Examples of EUV patterned contacts for 2 types of hard mask: TiN metal on a 32nm node relevant SRAM [5] and amorphous carbon (a-C) on a 22nm node relevant SRAM. The average in-line measured contact diameter is quoted.

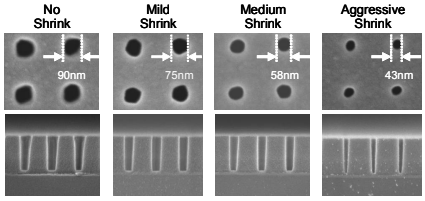

Fig. 3: Representative contact CD results (post-etch/ash), using a plasma assisted shrink process as part of the etch sequence [6]

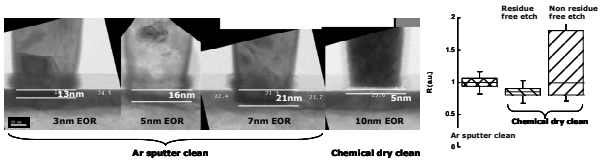

Fig. 4 (Left) Impact of the preclean process on the recess into the silicide for Ar sputter clean characterized by equivalent removal on blanket oxide (EOR) as compared to a chemical dry clean process. (Right) Sensitivity of the dry clean process to non-residue free patterning.

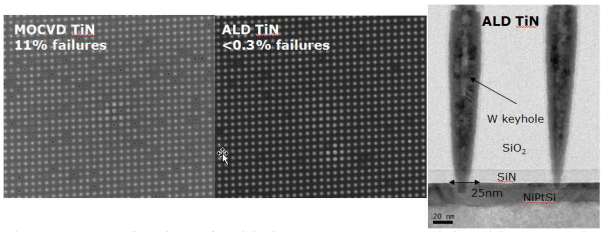

Fig. 5. Lower fraction of voided contacts on W module with ALD TiN compared to MOCVD TiN on contacts measured in-line to be ~31nm and ~25nm opening upon entering silicide. W filling is done with an ALD/CVD process using B_2H_6 as reducing agent in the ALD process.

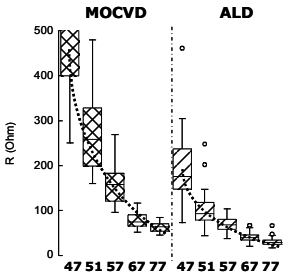

Fig. 6. Kelvin contact resistance as a function of in-line measured contact diameter for W modules with MOCVD and ALD TiN barrier on PVD Ti. The curved line is a guide to the eye.

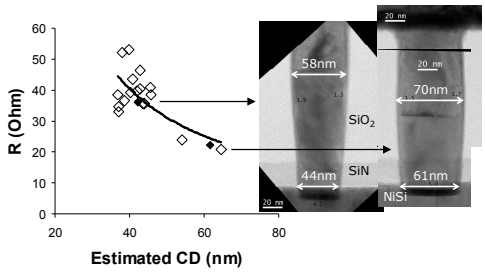

Fig. 8. Contact resistance as a function of in-line measured contact diameter for a Cu modules with PVD Ta(N)/ALD TaN bilayer barrier. The curved line is a guide to the eye. TEM images indicating the fill performance for 2 sample points in the resistance vs CD distribution.

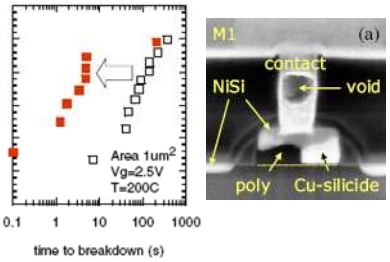

Fig. 9. (Left) TDDB lifetime distributions on p+poly on n-well capacitors at 200°C. Open symbols: robust barrier, closed: defective barrier. (Right) FIB cross-section failure analysis on a sample with low TDDB lifetime indicating formation of Cu silicide and Cu drift towards the gate oxide.

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