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Effect of Via-Profile on the Via reliability in Scaled-down Low-k/Cu Interconnects

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Introduction

In order to reduce power consumption and signal propagation delay in 40 nm-node LSI and beyond, porous low-k films with k-value (dielectric constant) less than 2.6 is introduced into Cu dual damascene interconnects (DDIs). Introduction of the porous low-k faces a big challenge to suppress process-induced damages, or increasing the k-value, during the DD integration process such as etching, metallization, and CMP [1-4]. From a viewpoint of the reliability, the DD via-profile in low-k films has a critical impact especially on the stress induced voiding (SiV). For example, it is reported that the SiV was promoted by the fenced-vias [5].

In this study, we investigate the effect of the via profile on SiV in the full-low-k/Cu DDIs. Three types of the non-fenced vias are prepared; i.e., (1) shallow-tapered, (2) stepped, and (3) deep-tapered vias with the via-bottom diameter of 70nm. It is found that the shallow-tapered and the stepped vias achieve high endurance against the SiV due to relaxing the stress gradient at the via bottom.

2. Experimental

Two types of low-k films were integrated into Cu-DDIs (Table 1); i.e., a molecular-pore-stack (MPS) SiOCH (k=2.5)[3,4] and a conventional rigid (r-) SiOCH film (k=3.0) as a reference. Fig.1 shows the concept of profile control in the via-first DD etching process with the SiO_2 hard-mask, which will be removed by CMP. On the trench patterning, the via-hole has been filled with the photo-resist to planarize the top surface for the trench lithography. The via profile is controlled by adjusting the level of the resist in the via hole. Here, the shallow-tapered, stepped, and deep-tapered vias were prepared with controlled bottom- diameter of 70nm-ϕ for all structures. After the Cu metallization and the Al probing pad formation, the inter-layer capacitance and the via resistance were measured. For the SiV test were used the via-chain patterns, in which the isolated vias (V1) were sandwiched between the lower (M1) and the upper (M2) lines of the widths from 0.14 μm to 3.0 μm. The wafer was stored in an oven at 175°C for up to 1000 h, and 10% increment of the via resistance to the initial one was defined as the SiV failure.

3. Results and Discussion

(a) Electrical Properties:

Fig. 2 shows the inter-line capacitance (C_{int}) of the 200nm-pitch lines in the MPS- and r-SiOCH films. The C_{int} in the MPS-SiOCH is 15% less than in the r-SiOCH, which is consistent with k-values of the as-deposited films. The TDDB lifetime was identical to each other (Fig. 3). These facts indicate that the via-first DD etching sequence with O_2-palsma ashing for the resist removal gives no sever impact on the film properties of the MPS-SiOCH due to the carbon-rich composition. Therefore, we were able to focus just on the control of the DD etching profile in the MPS-SiOCH film.

The inter-layer capacitance between M1 and M2 was almost identical irrespective of the via profiles, indicating that the trench depth was precisely controlled for all profiles in the full MPS-SiOCH film without the etch-stop layer (Fig. 4). The yields of the 70nm-ϕ vias in the 2M via-chains were 100%, and. the via resistance, or essentially the via bottom-diameter, was also identical irrespective of the via profiles (Fig. 5). Namely, the DD profiles such as the trench depth, the via height, and the bottom-diameter were controlled identically in the MPS-SiOCH film. The via-shape-profile is only a parameter for the SiV evaluation.

(b) SiV Reliability:

Fig.6 shows the SiV failure rate as a function of the line widths of M1 and M2 lines. As for the 0.14 μm-wide M1, the SiV was suppressed for all types of the via profile irrespective of the M2 width. (Fig. 6(a)) In the case of the 0.14 μm-wide M2 line, the failure rate of the deep-tapered via with the 3μm-wide M1 lines was 20%, however, the shallow-tapered and the stepped vias revealed no failure almost in all M1 width (Fig. 6(b)). The deep-tapered via after the SiV test revealed a wedge void in the wide M1 line under the via, where a grain boundary existed as a vacancy pipeline (Fig. 7).

The SiV test convinces that the failure probability of the M1 mode depends strongly on the via-profile, which might impact on the mechanical stress around the via.

(c) Stress Simulation:

The dependence of the via profiles on the SiV was confirmed by FEM simulation (Fig. 8). The stress gradient was estimated as a function of the taper angle θ and the taper depth of the vias. Here, the stepped via has the taper angle $\theta=90^o$ with the wide top-opening. The maximum stress gradient under the via decreases with increasing θ, and saturates over $\theta=45^o$ (Fig.9). When the taper reaches the via bottom to become the deep-tapered profile, however, the stress gradient increases to be the highest. These results explain the reason why the deep-tapered via promoted the SiV under the via.

Namely, the reduction in the stress gradient under the via is achieved by (1) the tapered profile at the top of via and (2) the vertical profile at the via bottom. The top taper angle is preferred to be over 45^o for reduction of the stress gradient, or essentially the SiV failure.

4. Conclusions

The shallow-tapered and the stepped vias improve the SiV reliability in the full-MPS/Cu DDIs, as compared with the deep-tapered via. The precise control of the via profile has become very important to keep the via reliability for 40nm nodes and beyond.

References

[1] M. Ueki, et al, IEDM2008 pp619 (2008). [2] M. Ueki, et al., Japanese J. Appl. Phys. 48 (2009) 04C029. [3] N. Inoue, et al., Jpn. J. Appl. Phys. Vol. 47, No. 4, p. 2468, 2008. [4] Y. Hayashi, et al., IEEE TRANS. SEMICON. MANUF., VOL. 21, NO. 3, p469, 2008. [5] H. Ohtake, et al, SSDM2005, pp300, (2005).

Table 1 Film properties of Low-k film.

	MPS*	rigid SiOCH
k-value	2.5	3.0
CTE (ppm/K)	35	11
Modulus (GPa)	3.5	13
Density(g/cm^3)	1.2	1.5
Composition Si:O:C	1:0.8:2.7	1:1.6:0.6
pore size (nm)	0.4	--

*Molecular Pore Stacking SiOCH

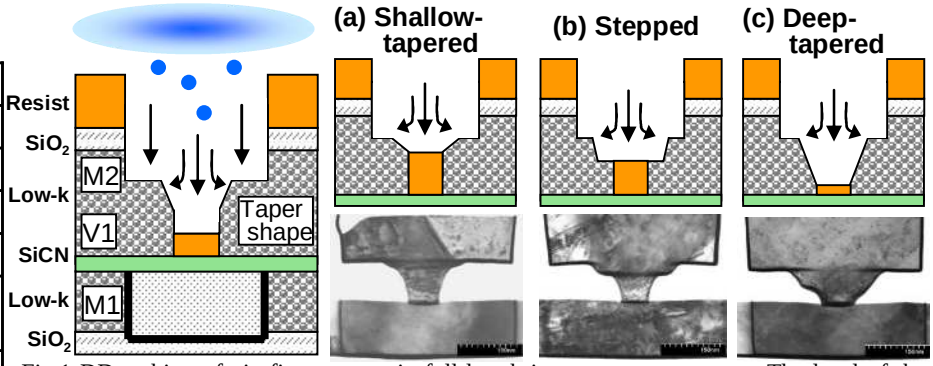

Fig.1 DD etching of via first process in full-low-k interconnect structures. The level of the resist in the via hole during the DD etching determines via profile, (a) shallow-tapered profile, (b) stepped profile, and (c) deep-tapered profile.

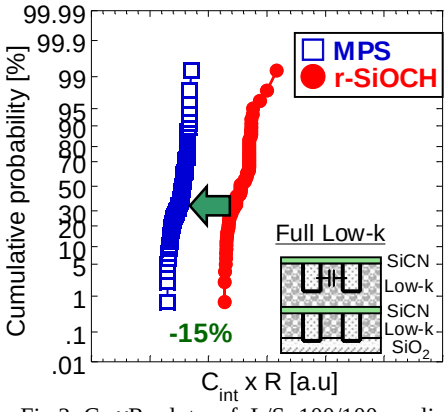

Fig.2 C_{int}xR plots of L/S=100/100nm lines. The interconnects with full-MPS (k=2.5) shows 15% lower C_{int} than with full rigid(r-) SiOCH (k=3.0).

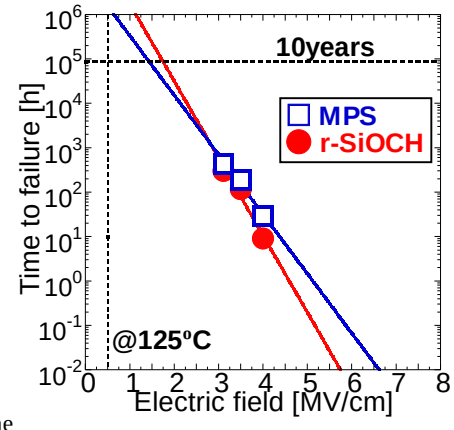

Fig.3 TDDB lifetime of full-low-k/Cu DDIs with MPS or r-SiOCH.

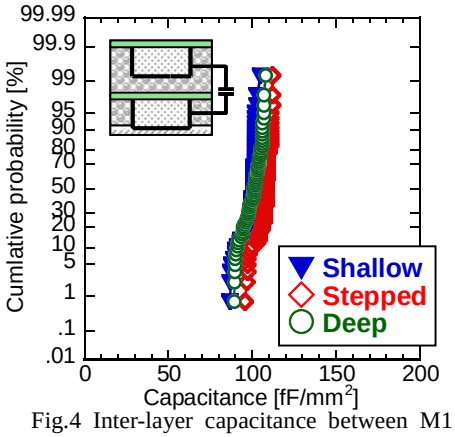

Fig.4 Inter-layer capacitance between M1 and M2. The interconnects with various via profiles show similar capacitance value.

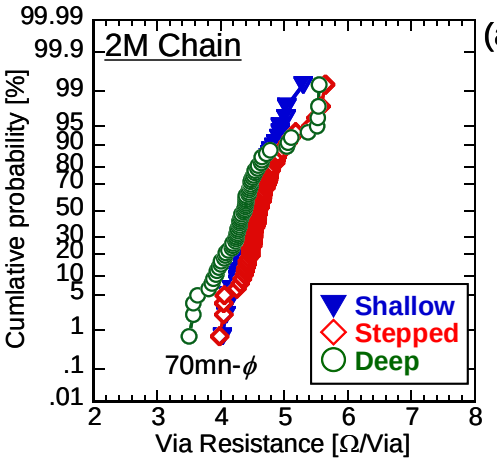

Fig.5 Distributions of the via resistance in 2M via chain with various via profiles.

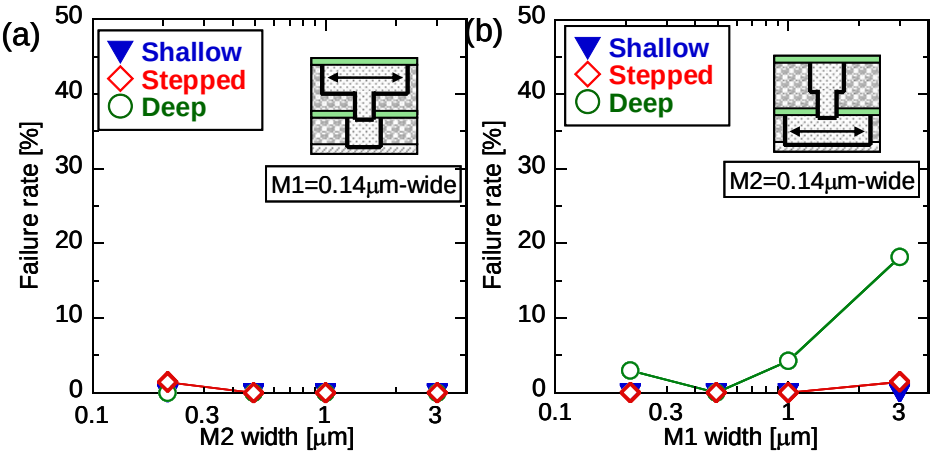

Fig.6 Failure rate of the via chain of various via profiles after SiV test; (a) the dependence on the M2 width, and (b) on the M1 width.

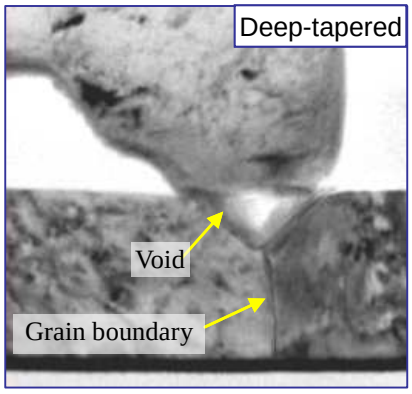

Fig.7 Cross-sectional TEM image of the failure analysis after the SiV test. The void is observed under the via.

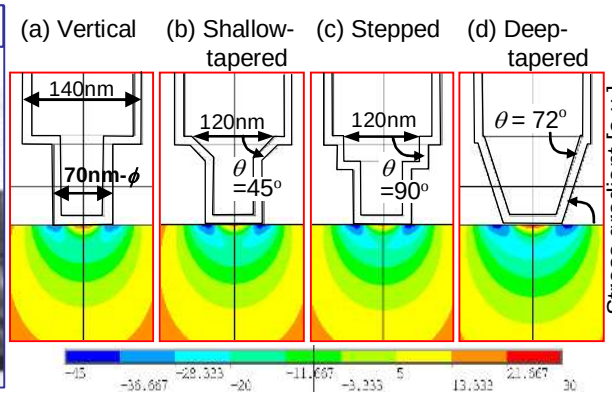

Fig.8 Stress simulation for various via profiles. The stress is simulated by FEM at the test temperature (175°C). Here, the stress in Cu is assumed to be relaxed at 350°C during the Cu annealing.

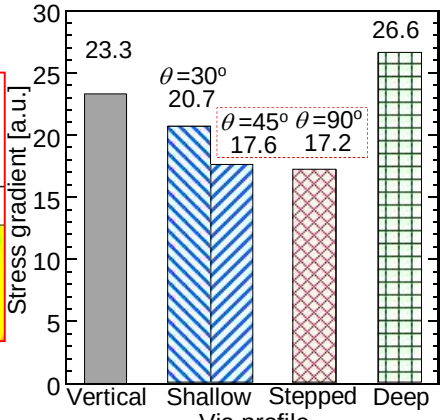

Fig.9 Stress gradient under the via as a function of via profile, resulted from the simulation.