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On the reliability of Cu contacts for the 32nm technology node and beyond

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Abstract

The reliability of devices with Cu contacts for various contact dimensions and diffusion barriers is studied. A methodology to evaluate these contacts is developed and concluded that an ALD barrier layer is required. Furthermore excellent barrier reliability on devices with 55nm Cu contacts is presented.
(Keywords: Cu contacts, diffusion barrier, reliability)

Introduction

The concept of Cu contacts is being considered for advanced technology nodes due to advantages related to lower contact resistance and reduced tool cost [1-3]. In this paper, we present a methodology to evaluate the reliability of Cu contact devices, screen various barrier technology options and benchmark to W contact devices.

The devices used in this paper were nMOS with 1.2nm SiO_2 gate dielectric. The tested Cu contacts range from 150nm (130mm node) with 28nm PVD TaN/Ta barrier down to 55nm contacts (32nm node) with a PVD Ta/ALD TaN barrier and a W reference (Table 1). The performance and yield data were obtained for at least 167 devices across 300mm wafers to verify the uniformity of the process.

The obtained contact chain yield for various barriers on 90nm (Fig. 1) and 65nm (Fig. 2) contacts demonstrates the need for an ALD TaN barrier layer when scaling Cu contacts [4]. The inset in Fig. 2 shows a Cu contact with 44nm bottom (58nm middle) dimension and excellent Cu filling behavior with this barrier.

Structures and monitors

There are two main failures mechanisms for Cu contacts. Voiding, leading to an open (especially in high aspect ratio S/D contacts), or the diffusion of Cu which in most cases destroys the device (Fig. 3a). Special test structures were designed to distinguish between these mechanisms: capacitors with various numbers of gate contacts on top of poly to assess if oxide breakdown is related to the contacts (Fig. 3b) and transistors with 1, 2, 4 or 5 S/D contacts to study the properties of high aspect ratio S/D contacts (Fig. 3c). As monitor for the contacts the gate leakage current (IV, It) and in case of transistors also the Ion/Ioff ratio is used.

Yield analysis, electrical and thermal stress

The distribution of gate leakage current for devices with 90nm Cu and W contacts in Fig. 4a demonstrates that the gate oxide yield is not affected by Cu. This observation holds for all splits (Table 1) verifying that shallow gate contacts are less affected by voiding. For devices with 5 S/D contacts the performance with Cu and W is similar (Fig. 4b) and the variations in median I_{ON}/I_{OFF} (Table 1) are mainly due to silicide variations.

A key challenge for Cu contacts is the reliability of the diffusion barrier [5-7]. The various test structures were exposed to constant voltage stress at 200°C to enforce the Cu diffusion but time-to-breakdown distributions revealed no contact related failures (Fig. 5a). The barrier stability under high temperature (400°C) was verified as well, proving the suitability of Cu contacts for a multi-level thermal budget (Fig. 5b).

Failure analysis and implications

Dedicated contact failure analysis is tricky because in contact chains the failure cannot be located and on multiple S/D contact transistors high yield is obtained (Fig. 6). The solution is to use transistors with single S/D contact. An Ion/Ioff yield map provides information if the failures are randomly distributed (Fig. 6) or related to a specific process step. Using the technique developed for detecting the breakdown spot position in gate oxides [8] it is possible even to predict whether the source or drain contact fails (Fig. 7). This enables precise failure analysis. An example is shown using FIB for the 5nm PVD Ta only barrier, which indeed revealed partial voiding (Fig. 8a) and diffusion of Cu on the sidewall into the PMD oxide (Fig. 8b) as cause.

From these results it is concluded that single contact devices with the proposed method are well suited for studying the failure mode. Furthermore, it shows that Cu encapsulation by the conventional PVD Ta(N) barrier is scaling limited. Therefore it was replaced by a bilayer barrier consisting of PVD Ta base layer and an ALD TaN top layer. The PVD Ta base layer ensures good contacting to the silicide and serves as a template for growth of a low-resistive ALD TaN layer at the contact bottom. Besides, the poor sidewall step coverage of the PVD Ta layer can be repaired by the quasi-conformal ALD TaN film. For adhesion to PVD Cu seed a 1nm PVD Ta flash layer is applied.

Reliability of 55nm Cu contacts

Approaching the required contact size for a 32nm process, in Fig. 9 the I_{on}/I_{off} for the 55, 65 and 80nm contact devices show reduced yield with the smallest contacts but no significant difference if the best performing devices are considered. After excluding time zero failures for the 55nm contacts, the TDDB distributions measured at 200°C show no indication of intrinsic reliability loss. Moreover, adding the η values for 55nm and 65nm contacts obtained at 2.5V to the voltage extrapolation, data show improved reliability compared to the PVD only barrier and coincide with the W contacts.

Conclusions

These data clearly show that for advanced nodes Cu contacts are a promising candidate and the required reliability can be ensured if the correct barrier approach is selected. Furthermore we present a method using single contact devices to assess potential failure modes and demonstrate excellent intrinsic reliability of devices with 55nm Cu contacts.

Acknowledgements

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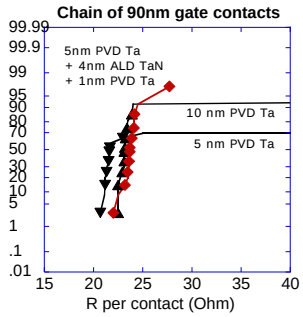

Fig. 1 On 65nm node contacts, yield drops for PVD Ta barrier thicknesses below 10nm. This can be avoided by the introduction of an ALD TaN quasi-conformal layer.

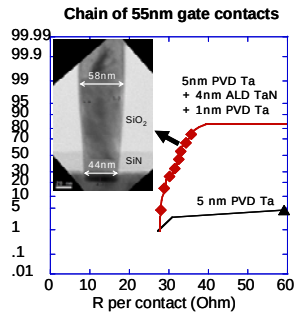

Fig. 2 At 32nm node, the ALD layer is the enabler for reliable metallization. The inset is showing the excellent filling behavior obtained with this barrier.

Node (contact size)	Cu barrier	Tested contact size (nm)	Yield (VG>0)	Yield (VG<0)	Median Ion (A/µm)	Median Ioff (A/µm)	Remarks
130nm (150nm)	28nm PVD TaN/Ta	150	164/167	165/167	0.68e-3	2e-8	Barrier not scalable towards 32nm node
65nm (90nm)	28nm PVD TaN/Ta	90	162/167	162/167	0.57e-3	0.67e-8	
		80	165/167	165/167	0.88e-3	40e-8	
32nm (50nm)	5nm PVD Ta	90	164/167	164/167	1.3e-3	0.29e-8	Low contact chain yield
	5nm PVD Ta + 4nm ALD TaN + 1nm PVD Ta	90	167/167	167/167	1.1e-3	0.07e-8	Only ALD TaN with sufficient sidewall coverage
		65	162/167	163/167	1.05e-3	30e-8	
		55	165/167	165/167	1e-3	5e-8	
W reference		90	165/167	165/167	0.63e-3	1.5e-8	1.5e-8

Table 1 Summary of the measured nMOS devices with 1.2nm SiO_2 gate oxide thickness. For different diffusion barriers the contact sizes range from 55 to 150nm. The gate leakage yield and median Ion/Ioff values are mentioned aswell.

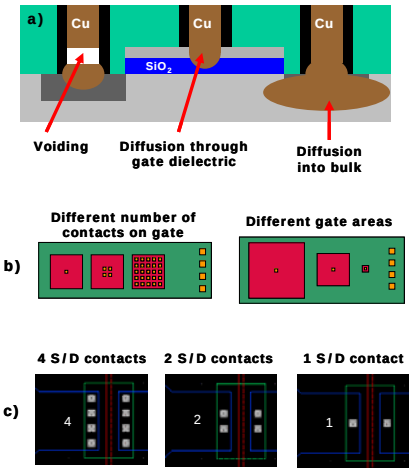

Fig. 3 Contact failure mechanisms (a) and dedicated test structures for gate (b) or S/D (c) contacts.

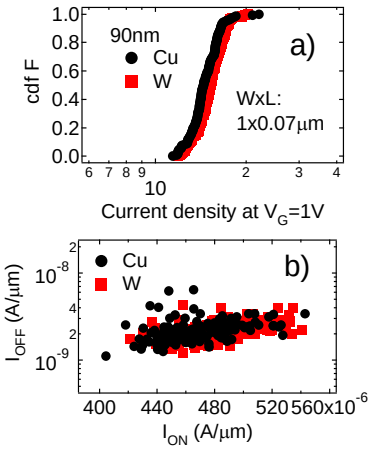

Fig. 4 For these 90nm contact devices comparing Cu vs W no difference in gate leakage or Ion/Ioff is observed.

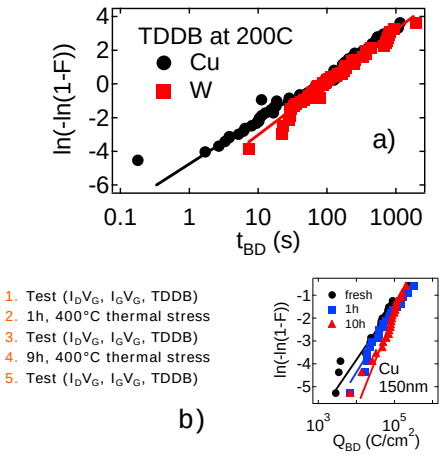

Fig. 5 High temperature electrical (a) and thermal only stress (b) were used to evaluate the reliability of the different barriers and for benchmarking with W.

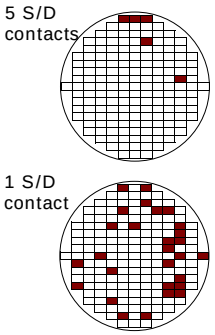

Fig. 6 Ion/Ioff yield map for the 5nm PVD barrier devices with either 5 or 1 S/D contacts.

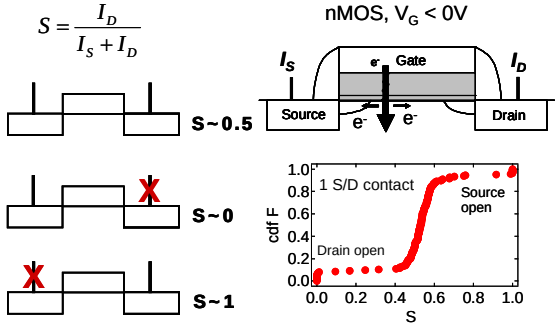

Fig. 7 Methodology to detect individual failing contacts. Electrons diffuse to the extensions and from the ratio S it is possible to predict whether source or drain fails. The data correspond to the devices shown in Fig. 6.

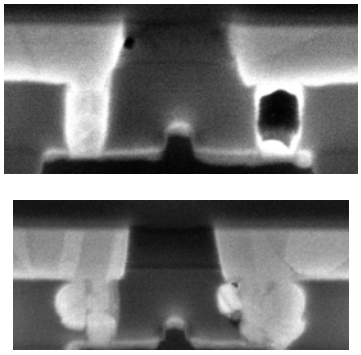

Fig. 8 Physical characterization of failures using single contact devices where voiding or diffusion at the sidewalls is observed.

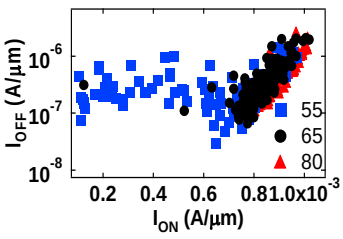

Fig. 9 Performance with 55, 65 or 80nm contacts. Especially for the 55nm devices the Ion is reduced due to insufficient contact filling.

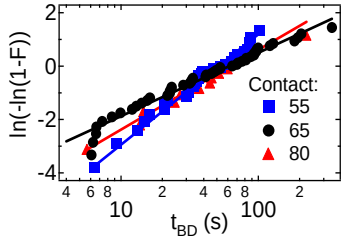

Fig. 10 TDDB distributions measured at 200°C and 2.5V for the small Cu contact devices reveal no intrinsic reliability difference.

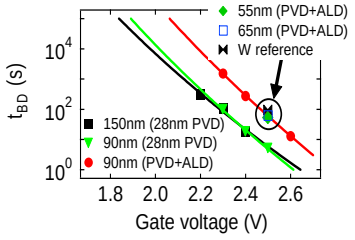

Fig. 11 Voltage acceleration plot for 90 and 150 nm Cu contacts. Adding the values measured at 2.5V for the smaller contacts show no degradation in lifetime.

References

[1] Demuynck, IITC, 2006
[2] Islam, VLSI, 2000
[3] Inohara, IEDM, 2001
[4] Demuynck, AMC, 2007
[5] Vd Bosch, IEDM, 2006
[6] Seo, AMC, 2008
[7] Kauerauf, AMC, 2008
[8] Degraeve, IRPS, 2001