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A Comparison of Lifetime Improvements in Electromigration between Ti Barrier Metal and CVD Co Capping

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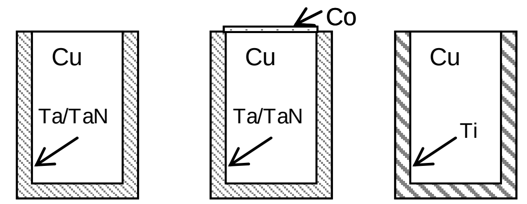
1. Introduction

To achieve highly reliable Cu interconnects, applications of Cu alloy interconnects and metal capped Cu interconnects have been proposed. Cu alloy interconnects are fabricated by doping impurities from a Cu alloy seed layer or a barrier metal layer. As metal capping on Cu interconnects, Co-main cap metals have been studied frequently. The difference of these process technology seems to cause a difference in electromigration (EM) improvement characteristics. In this study, EM lifetime of Cu interconnects using Ti barrier metal or CVD Co capping were compared and the effects of impurities on Cu diffusion was investigated. It was proposed that suppressing Cu diffusion thorough the grain boundaries on the Cu surface is effective for lifetime improvement in EM.

2. Experiment

Two-layer Cu interconnects (M1/via/M2) with 55nm-node technology were used in this study. Three different structures of Cu lines were prepared for M1 as shown in Fig. 1, which were using (a) conventional pure Cu seed and Ta/TaN barrier metal (Cu/Ta/TaN), (b) Co CVD cap metal (Co/Cu/Ta/TaN)[1], and (c) Ti barrier metal (Cu/Ti) [2]. As the inter-layer dielectrics, SiO_2 was used for M1, and a CVD low-k film was used for via and M2 levels. As the dielectric capping layer, SiCN was deposited on Cu or Co CVD cap metal of M1.



(a) Cu/Ta/TaN (b) Co/Cu/Ta/TaN (c) Cu/Ti

Fig.1 Schematic of Cu lines of (a) Cu/Ta/TaN, (b) Co/Cu/Ta/TaN and (c) Cu/Ti.

An EM test structure of multi-link type [3] was used in this study. The test structure consisted of 20 segments terminated with vias and the downstream EM lifetime was evaluated. Both the M1 line width and the via diameter were 90nm. The M1 line length was 100μm. EM test conditions were the current density of 6 MA/cm^2 and temperatures of 250, 275, 300, and 350 ^oC. Resistances of 90nm width lines were measured at room temperature and at 20 K to investigate the scattering factors for electrons, e.g., impurities (Ti or Co) or grain boundaries in Cu lines, by the residual resistance ratio ($RRR=R_{RT}/R_{20K}$). In this study, R_{20K} was used as the residual resistance (R_r). Ti or Co in Cu lines were investigated by cross-section TEM imaging and EDX analysis. Cu grains in Cu lines were observed by plan view TEM imaging.

3. Results and discussion

Effects of Ti barrier metal or Co cap metal on EM lifetime

Fig. 2 shows the temperature dependence of EM lifetime. Cu/Ti and Co/Cu/Ta/TaN improved EM lifetime significantly compared with Cu/Ta/TaN. Activation energy (Ea) of EM lifetimes can be extracted from the slope of the fit lines, which were found to be around 1.1eV for Cu/Ti and Co/Cu/Ta/TaN, and 0.92eV for Cu/Ta/TaN. The higher Ea values of Cu/Ti and Co/Cu/Ta/TaN indicate that Cu diffusion was suppressed by them, compared with Cu/Ta/TaN. Fig. 3 shows SEM images of EM failure voids. As these EM failure voids were generated under the via at the cathode end of Cu lines, it is suggested that the failure modes were similar in those Cu lines in spite of the difference in lifetimes.

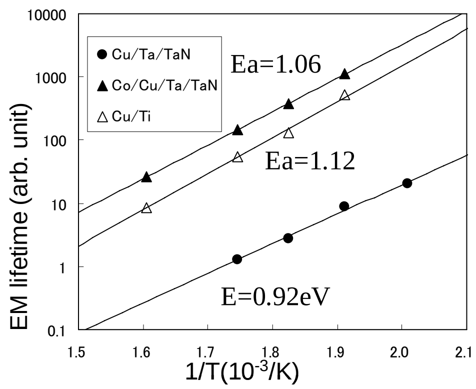
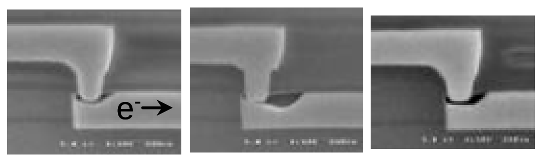


Fig. 2 Temperature dependence of EM lifetime.



(a) Cu/Ta/TaN (b) Co/Cu/Ta/TaN (c) Cu/Ti

Fig. 3 Cross-section SEM images of EM failure voids.

Effects of Ti or Co

The contribution of Ti or Co atoms to the line resistance was investigated by RRR. Small RRR means large Rr,

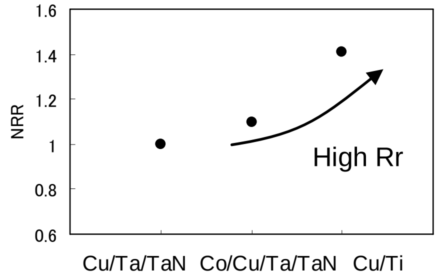


Fig. 4 Normalized RRR of 90nm width line.

which indicates the large amount of impurities in the Cu lines. Fig. 4 shows the Normalized Rr (NRR) [4] of each Cu line. Cu/Ti and Co/Cu/Ta/TaN show larger NRR than Cu/Ta/TaN and Cu/Ti shows larger NRR than Co/Cu/Ta/TaN. These results suggest that Cu/Ti includes more impurities (Ti) in the Cu line.

To investigate the distribution of impurities in the Cu lines, Ti and Co were observed by TEM and EDX analysis. Fig.5 shows cross-section TEM images and EDX data of Cu/Ti and Co/Cu/Ta/TaN. As shown in Fig. 5 (a), much Ti was detected at the grain boundary on the Cu surface (position 2) and a small amount of Ti was detected at the grain boundary in the Cu line (position 6). However Ti was not detected on and in the Cu grain. It is indicated that Ti existed mainly at the grain boundary on the Cu surface. In Fig. 5(b), Co was not detected in the Cu line and a small amount of Co was detected at the Cu/Ta interface (position 3,6). The result of EDX analysis agreed with the result of Rr.

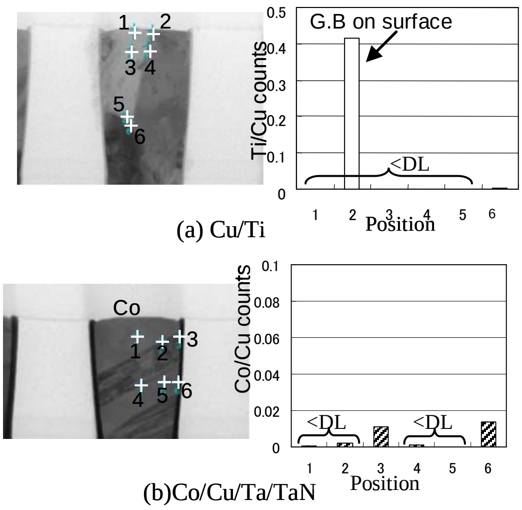
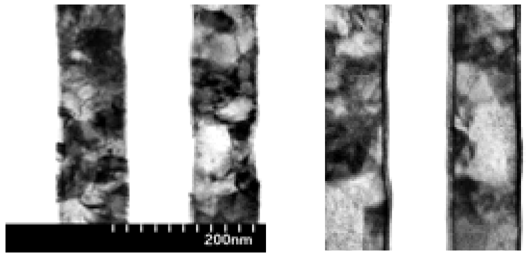


Fig. 5 Cross-section TEM images and EDX data of 90nm width line.(a) Cu/Ti and (b) Co/Cu/Ta/TaN.

Fig. 6 shows the plane view of TEM photographs of Cu/Ti and Cu/Ta/TaN. The Cu grain size of Cu/Ti is smaller than that of Cu/Ta/TaN and more grain boundaries exist on the Cu surface and in the Cu line. The Cu grain boundaries along the length of the line are observed, which are likely to become Cu diffusion path by EM [5].

The EM improvement effect of Cu/Ti was speculated from these experimental results as shown in Fig. 7. As shown in Fig. 5, Ti atoms exist mainly at the grain boundaries on the Cu surface. These Ti atoms suppress Cu diffusion through the grain boundaries on the Cu surface, which leads to the high Ea and the long EM lifetime. In the case of Co/Cu/Ta/TaN, Co capping suppresses Cu diffusion through the whole Cu surface including the grain boundaries. In addition, the density of the grain boundary is lower than that of Cu/Ti, which means fewer diffusion paths. Therefore, EM lifetime of Co/Cu/Ta/TaN is somewhat longer than that of Cu/Ti.



(a) Cu/Ti (b) Cu/Ta/TaN

Fig. 6 Plan-view TEM images of 90nm width line. (a) Cu/Ti and (b) Cu/Ta/TaN.

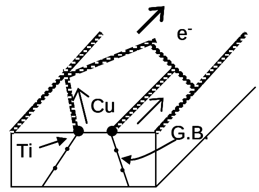


Fig. 7 EM improvement model for Cu/Ti.

4. Conclusion

Cu/Ti and Co/Cu/Ta/TaN showed notable EM lifetime improvement comparably, though Ti existed mainly at the grain boundaries on the Cu surface while Co covered whole the Cu surface. The suppressing Cu diffusion through the grain boundaries on the Cu surface is significantly effective for the improvement of EM reliability. Strengthening grain boundaries on the Cu surface is important for achieving highly reliable interconnects.

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