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Recent Progress in High-Resolution and High-Speed CMOS Image Sensor Technology

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1. Introduction

Required technologies to build a high resolution CMOS image sensor and a high-speed (or high-frame rate) CMOS image sensor are basically the same. For example, the data rate of a 10M-pixel, 60 frames/s (fps) image sensor is almost equal to that of a 1M-pixel, 500 fps image sensor. In this paper, we will describe advantages of the CMOS image sensor over the CCD image senor in view of the high-resolution, high-speed imaging and associated design challenges in the CMOS image sensor. An 8.9M-pixel CMOS image sensor that we have developed is reviewed as an example of high-resolution, high-speed image sensors, and future prospects are given.

2. CMOS Image Sensor and CCD Image Sensor

The CMOS image sensor and the CCD image sensor are the dominant imaging devices. For high-speed camera applications, the CMOS image sensor is a technology of choice since it can offer high frame rates with much lower power consumption. Representative configurations of the CMOS image sensor and the CCD image sensor are shown in Fig. 1. A video signal of the CMOS image sensor is obtained by selecting a pixel in an "x-y addressing" scheme. A digital output scheme has become popular since signal processing circuits, such as an amplifier, an analog-to-digital converter (ADC), can be integrated on-chip in the CMOS process. On the other hand, the CCD image sensor provides excellent image quality with very low fixed pattern noise (FPN) and no image distortion (which can be seen in the CMOS image sensor due to its x-y addressing scheme). However, all the charge transfer gates need to be driven all the time and high voltages are needed to secure high charge transfer efficiency. Therefore, it is inherently difficult to reduce power consumption in the CCD image sensor. This is particularly true with a large format array for a high-end use. Although large FPN caused by the variations in electrical properties of the pixel circuit was considered as a big problem of the CMOS image sensor, imaging performance of the CMOS image sensor has reached a level to be comparable to that of the CCD image sensor, thanks to recent technology developments [1]-[3].

3. High-Speed CMOS Image Sensors

The representative three types of pixels are shown in Fig. 2 [4]. A 3-transistor PD pixel, shown in Fig. 2(a) is suitable for high-speed operation because a charge transfer sequence (that is needed for 4-transistor pixel) is not needed. However, the reset noise (or kT/C noise) associated with the photodiode reset cannot be removed and the photodiode leakage current is relatively large. A 4-transistor pinned photodiode (PPD) pixel is the most popular pixel and is shown in Fig. 2(b). It offers extremely low noise property due to the complete charge transfer from PPD to the floating diffusion (FD; the charge sensing node inside a pixel) and the reset noise suppression by the correlated double sampling (CDS). In addition, the photodiode leakage current is inherently low due to its buried PD structure that was first introduced to the CCD pixel [5]. Shown in Fig. 2(c) is a "frame shutter" (or "global shutter") pixel and is used for applications where the charge integration period/ timing needs to be identical for all the pixels in the imaging array. The "frame shutter" is realized by adding an analog memory inside a pixel.

An on-chip analog-to-digital conversion for high-resolution and high-speed CMOS image sensors is most often implemented in a column-parallel fashion. An effective conversion rate is increased by many ADCs operated in parallel, while each ADC's conversion speed is moderate. For example, the pixel rate is 1Gpixels/s when a 1000×1000 pixel image sensor operates at 1000 fps. If 1000 ADCs are equipped, the conversion rate of each ADC is 1MHz. The column-parallel ADC requires small area and low power consumption. A single-slope ADC [1], a successive approximation (SA) ADC [2][6] and a cyclic ADC [3] are used.

The output interface is also an important building block, since a huge amount of high-speed data stream needs to be output from the high-resolution, high-speed image sensor. Adopting a high-speed serial interface is a recent trend [6][2] to reduce the number of output pins and power consumption and to suppress noise induced from a output pattern dependent fluctuation on the power supply.

4. Digital-Output CMOS Image Sensor for UDTV Applications

Fig. 3 shows a block diagram of a 1.25-inch, 8.9Mpixel CMOS image sensor that we have developed[2]. This image sensor is designed to meet the ITU-R's UHDTV1 standard [7] and thus operates at 60 fps with 12 bit digital output. It also meets the 4000 line digital cinema format. To achieve low noise performance to meet requirements for a broadcasting use, the 4-transistor pinned PD pixel is used. The on-chip ADC is a 14 bit SA ADC of which conversion time is 1.7μs and is placed on the top and bottom sides in double the column pitch. Prior to the ADC, a pre-amplifier of which maximum gain is 8 is implemented. To remove possible variations of ADC offsets over time (including possible temperature changes), a digital CDS scheme [1] is adopted, where two signals, before and after the charge transfer from PPD to FD, are digitized and subtracted. The dual memory bank architecture allows a pipelined processing of the A/D conversion and the digital data readout from the second memory bank. The high-speed low-voltage differential serial interface with the common-mode voltage of 200mV and the differential signal amplitude of 200mV$_{p-p}$ at a termination resistor of

100Ω is introduced. With these implementations, the maximum handling charge of 27ke$^-$ and the noise floor of 2.8e$^-$, the column FPN of 0.4e$^-$ at the maximum gain of 8, have been obtained. It is confirmed that the image sensor is applicable for a broadcasting use through evaluation of a prototype camera using a color version of this image sensor. [8] The specifications and performance of the 8.9Mpixel CMOS image sensor are summarized in Table I.

5. Future Prospects and Challenges

The application areas of high-resolution, high-speed image sensors are expanding, such as video modes in digital still cameras, higher resolution video cameras, digital cinemas and the next generation broadcasting systems like NHK(Japan Broadcasting Corporation)'s Super Hi-Vision systems. It is expected that the CMOS image sensor will play more and more important roles by achieving lower power consumption, lower noise and higher sensitivity. To realize a low noise frame shutter pixel is a challenge for high-speed industrial and instrumentation cameras.

References

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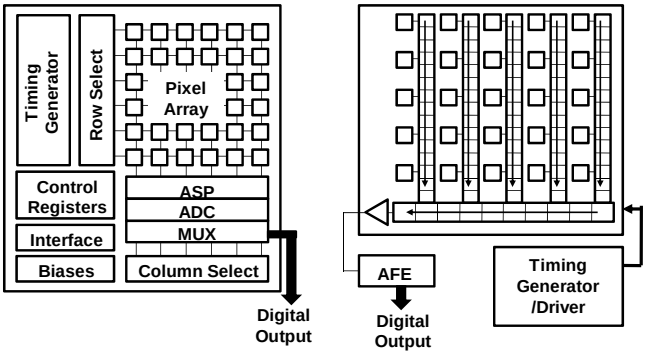
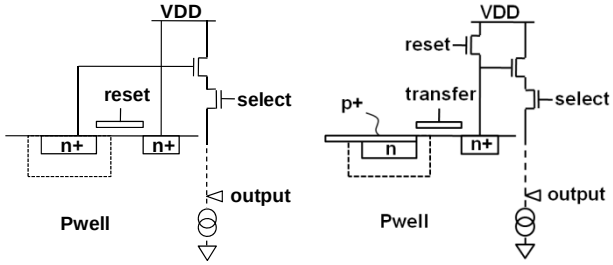
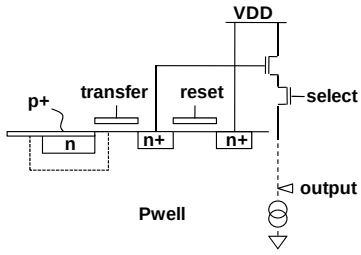


(a) CMOS image sensor (b) CCD Image sensor

Fig. 1 : Representative configurations of the CMOS image sensor and the CCD image sensor



(a) 3 Transistor pixel (b) 4 Transistor pixel



(c) Frame shutter pixel

Fig. 2 : Representative three types of pixels for the CMOS image sensor

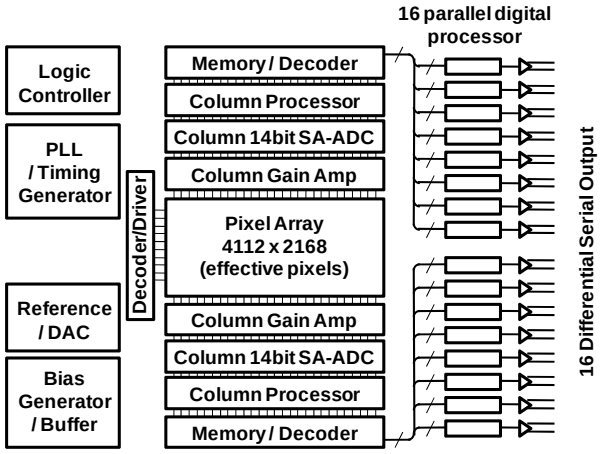


Fig. 3 : Block diagram of a 1.25-inch, 8.9Mpixel CMOS image sensor

Table I : UDTV sensor specifications and performance

Fabrication process	0.18mm 2Poly, 3Metal
Effective pixels	4112 (H) × 2168 (V)
Output	12bit (60fps), 14bit(50fps)
	16 lane differential serial interface
Max pixel output rate	792 Mpixels/s (12bit, 60fps)
Pixel conversion gain	45mV/e- at pixel diffusion
Linear full well	27.8 ke-
Readout temporal noise	2.8e- (max gain, 12bit, 60fps)
Row temporal noise	0.31e- (max gain, 12bit, 60fps)
Column FPN	0.36e- (max gain, 12bit, 60fps)
Total power consumption	1085mW (12bit, 60fps)