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A Reference CMOS Circuit Structure for Evaluation of Dynamic Voltage Variation in Power Delivery Networks

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1. Introduction

Accurate understandings of dynamic noises in power delivery networks (PDNs) of very large scale integration (VLSI) chips are strongly demanded, with diversified assembly structures. Power supply (PS) noise induces unexpected timing viorations among logic switching operations. Substrate crosstalk noise interfares with high-resolution analog and radio frquency (RF) signal processing as well as high-bandwidth communication channels in mixed analog and digital circuits. Such noises finally degrade system performance [1]. The issues have been traditionally concerned by integrated circuit designers, however, will become of higher significance among system designers intending advanced high-density wide-bandwidth packaging and assembly technologies.

PS noise results generally from the interaction of PS current with parasitic impedances of PDN in a digital circuit. Density as well as speed of logical switching operations are decisive factors determining the PS current. Materials as well as structures of assembly strongly govern the PDN impedances. Therefore, It is needed to draw a general way to evaluate PS noise of circuits across different technology generations and variations.

This paper proposes a reference circuit structure that can be universally implemented in CMOS technologies and is well understood with regard to dynamic PS noise generation.

2. Circuit Definition

A loop shift register (SR) circuit, shown in Fig. 1, has a cascade of D-type flip flop (DFF) cells where the output from the last DFF can loop back to the input of the cascade. A binary data sequence like "010101...01" is written into the cascade when the loop is opened. The sequence is shifted in a bit-by-bit way at every rise edge of a clock signal, Clk, and circulates in the cascade as long as the loop is closed. Here, DFF is normally found in a standard logic cell library of any CMOS technology.

The circuit behaves generally like a sequential logic circuit that is synchronous to a system clock, but with the shallowest logical depth. Therefore, switching activities internal to the loop SR circuit are intensively localized immediately after the clock edges where PS current experiences an obvious peak. This simplest logical structure eliminates the need of full-scale logic simulators for noise analysis. On the other hand, the size of PS current is dependent on devices, supply voltages, as well as strengths of PDNs. We can focus intensively on the technology dependences of PS noise generation by the loop SR circuit.

3. Simulation Models

PS noise generation of a loop SR circuit can be simply captured in an equivalent circuit model given in Fig. 2. A certain amount of charges are periodically drawn from an external power source with the clock interval of Tclk. PS current flows through impedances parasitic to PDN, which creates dynamic voltage variations on Vdd and Gnd paths, namely, PS noises. In addition, a p-type substrate, that is tightly connected to on-chip Gnd wirings in a CMOS technology, also experiences voltage variation known as substrate noise.

The amount of charges consumed by DFF cell is calculated as in Fig. 3, where a layout-parameter extracted transistor level netlist is simulated with SPICE circuit simulator. It should be noted that DFF cell contains internal logic toggles at every clock transitions, corresponding to the receipt of clock signals as well as the change in logic values to hold. This requires a table to be looked up in PS current simulation.

An entire equivalent circuit model of PS noise generation, given in Fig. 4, includes on-chip equivalent models as well as off-chip lumped components. On-chip part includes resistive meshes of Vdd wiring network as well as Gnd counterparts that are tightly connected to the resistive networks of a p-type substrate. The off-chip components represent electrical characteristics of packages and boards and are extracted through electro-magnetic field solvers or directly by network impedance measurements.

4. Measurements and Evaluation

We have evaluated PS noises of loop SR circuits in different CMOS technologies. A typical layout view of an array of loop SRs is given in Fig. 5, where DFF cells are regularly placed and routed in order to get maximally packed.

Time-domain noise waveforms that are measured as well as simulated on on-chip part of PDN of an array of loop SRs are given in Fig. 6(a), and the dependence of peak-to-peak noise voltage, Vpp, on the number of loop SRs simultaneously activated is also summarized in Fig. 6(b). The loop SRs were fabricated in a 0.18 μm CMOS technology and operated at the standard supply voltage of 1.8 V. Measurements were performed with on-chip noise monitors [2]. It is clearly shown that the simulation with the derived equivalent circuit models precisely captures PS noises both in wave shapes as well as noise voltages, in comparison with measurements.

The array of loop SRs was also fabricated in a 90 nm CMOS technology, with 1.2 V supply voltage. Figure 7 compares noise waveforms as well as Vpp trends obtained by measurements and simulation. It is shown that the correlation of measurements and simulation is

well maintained even with the scaled devices.

The higher amplitude of noises seen in Vdd than Gnd is due mainly to the difference in impedance seen from the circuits, where the larger number of pads connected to system ground strongly drains off the ground currents, with the help of a substrate network. The results are similarly explained for both technologies.

5. Conclusion

It was experimentally found that dynamic noise generation of CMOS digital circuits followed the general mechanism. Measurements and simulation of power supply and substrate noises with remarkable correlation were successfully achieved, with the loop SR circuits as reference structures for evaluation of dynamic noises in power delivery network.

References

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[2] M. Nagata, et al.,"Substrate Integrity Beyond 1 GHz,"*in Proc.IEEE Intl. Solid-State Circuits Conf. (ISSCC)*, pp. 266-267, 2005.

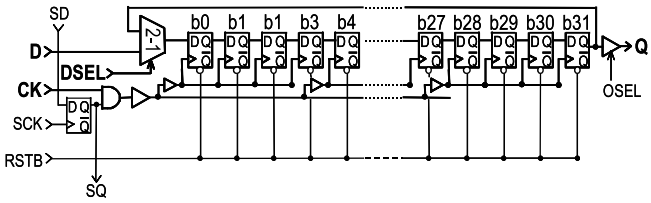

Fig. 1: Circuit schematic of a loop shift register (SR) circuit.

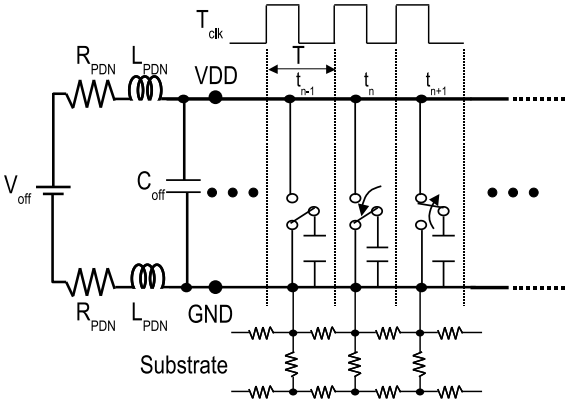

Fig. 2: Charge based modeling of noise generation.

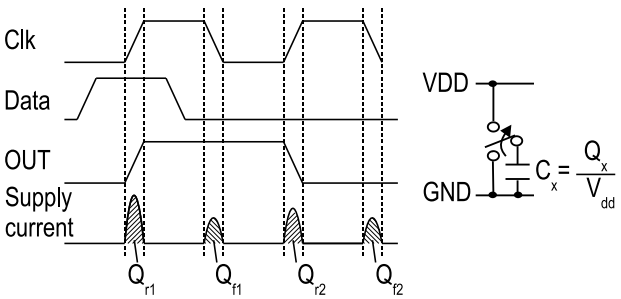

Fig. 3: Equivalent circuit extraction of DFF cells.

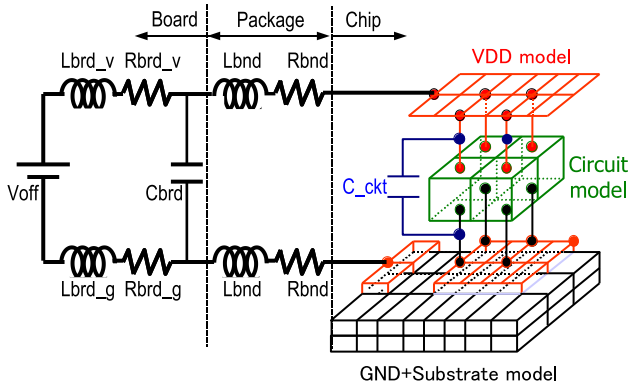

Fig. 4: Equivalent circuit for chip level noise simulation.

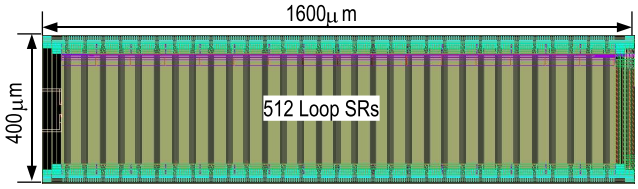

Fig. 5: Layout view of an array of loop SR circuits.

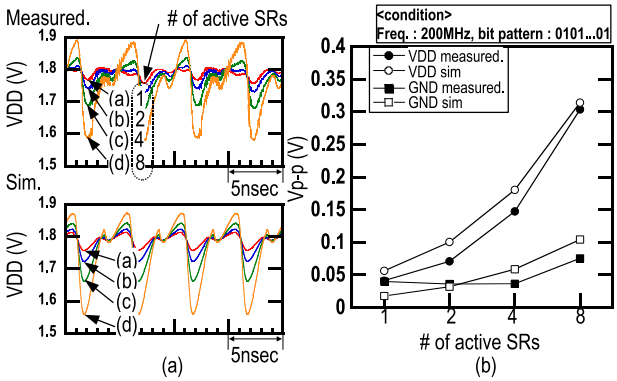

Fig. 6: Measurements and simulation of power supply and ground noise in 0.18 um CMOS technology. (a) Noise waveforms and (b) Vpp dependence on the number of active loop SRs.

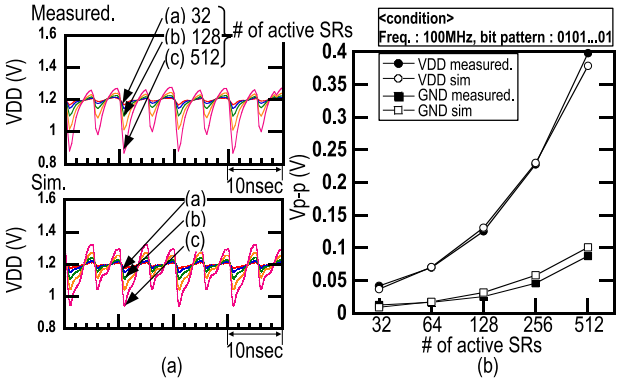

Fig. 7: Measurements and simulation of power supply, ground, and substrate noise in 90 nm CMOS technology. (a) Noise waveforms and (b) Vpp dependence on the number of active loop SRs.