Substrate Noise Analysis of Digital Circuits to Optimize Substrate-Contact Space

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Abstract—Substrate noise characteristics in digital circuits are analyzed to optimize the substrate-contact distance. For the analysis, a well resistance and capacitance model is developed. The optimal distance is varied according to the behavior of the operating circuit. When the transistors operate at the same time, like a clock (CLK) buffer, the substrate contacts have to be placed closely. On the other hand, when the transistors operate alternately, like circuits in a data path, the substrate contacts can be placed sparsely. By predicting the behavior of circuit operation, we can reduce the data path area by 10 % compared to that of the conventional design. The analysis is verified using 65-nm triple-well test chips.

I. INTRODUCTION

At an embedded SoC, a chip-area reduction is required to reduce a chip cost. As shown in Fig. 1, a large space of substrate contact reduces chip area. However, fewer substrate contacts increases substrate noise, which induces fluctuations in transistor switching speed and false operation. A timing design of SoC has a timing margin to prevent false operation. The timing margin is corresponding to the timing fluctuations caused by the substrate noise. Today, it is difficult to improve SoC performance with process shrinking. Therefore, a reduction of unnecessary margin is required in order to improve SoC performance. For reducing an unnecessary margin, we need an accurate estimation of the timing fluctuation caused by the substrate noise.

Substrate noise propagation from digital circuits to analog circuits is investigated by modeling and measurement [1]–[6]. However, an effective parameter to estimate a substrate noise in digital circuit is different from that of mixed-signal-chip substrate noise analysis. Because, in digital circuits, the distances between aggressor circuits and victim circuits are much smaller than that of mixed-signal chips. Adjacent transistors are aggressor circuits and victim circuit.

In mixed-signal-chip substrate noise analysis, a chip-level resistance, capacitance and inductance are effective parameter. And total current generated by digital-circuits switching is effective parameter [3]. However, to analyze substrate noise propagation from a transistor to adjacent transistors in a digital circuit, a finer transistor-level well resistance and capacitance (RC) are effective parameter. Moreover, each transistor switching condition is effective parameter.

Here, a well RC model considering a well device structure is introduced. We estimated how this model affects substrate noise estimation accuracy. By using this model, substrate noise characteristics in digital circuits are analyzed. This is determined by measuring the correlation of ring oscillator frequency and substrate contact space on a test chip.





A well RC model that represents transistor-level well resistance and capacitance connections correctly is required in order to accurately estimate substrate noise propagation between adjacent transistors. Fig. 2(a) presents a standard cell layout. Fig. 2(b) and (c) present a cross section with a conventional well RC model. Fig. 2(d) and (e) show a cross section with the well RC model of this work. This well RC model is composed of capacitances (source, drain, well) and well resistances. The substrate noise is mainly generated by switching of a drain capacitances. And the substrate

noise is absorbed by well parasitic capacitances and substrate contacts. The different points between a conventional model and our model are as below.

- The upper vertical resistance shows the influence of shallow trench isolation(STI). The existence of STI increases substrate noise. Because the value of resistance to the noise absorption increases.
- The lower vertical well resistance shows the effect of well resistance, which is increasing at an exponential rate in proportion to the well depth. High resistivity of a well bottom reduces the absorption effect of the well bottom parasitic capacitance, and substrate noise increases.

These effects of device structures increase substrate noise compared with a conventional well RC model.

Moreover, both nodes of a well side capacitance will be excited in the same voltage direction by the same drain node of a CMOS transistor. Therefore, the absorption effect of the well side capacitance reduces, and substrate noise increases. Fig. 3 plots the simulation results of both well RC models. The result of the well RC model introduced in this paper shows 30%-50% higher noise than the results of the conventional model. This indicates that vertical resistances and divided well capacitances are effective parameters to estimate substrate noise.





The substrate noise of each transistor is due to the substrate contact space and factors including the number of switching transistors, relative position, switching timing, and drain voltage switching to high or low. Fig. 4 shows the effect of switching timing and drain voltage. As shown in Fig. 4(a), If many transistors switching to same voltage at the same timing,

large substrate noise is generated because of the voltage amplitude effect. For example, large clock buffers placed adjacently generate substrate noise like this. To analyze this substrate noise amplitude effect and its correlation with substrate contact space, substrate noise was simulated by changing the number of switching inverters and substrate contacts space. The simulation results are plotted in Fig. 5. In Fig. 5(a), substrate noise of the center switching transistor is shown. Fig. 5(b) shows substrate noise of an adjacent transistor to the switching transistor in the center, which is not switching. Substrate noise of Pwell is indicated. Substrate noise of Pwell is larger than that of Nwell because the resistance of Pwell is higher than that of Nwell. At spaces greater than 13 μ m, substrate noise has no correlation with the distance from substrate contacts. This result shows that the distance which substrate contacts can suppress substrate noise, is shorter than 13 μ m. At distances greater than 13 μ m, the absorption effect of neighboring well parasitic capacitance on substrate noise determines the substrate noise peak value. At distances where substrate contacts are ineffective, substrate noise increases as the number of switching inverters increases. These results indicate that many transistors switching at the same time and in the same voltage, like a clock buffer, need adjacent substrate contacts in order to suppress substrate noise.

However, there is a substrate noise canceling effect, as shown in Fig .4(b). Transistors that switch alternately in different voltages, cancel each other's substrate noise. For example, data path circuits generate and cancel substrate noise in this way. To analyze this canceling effect, substrate noise was simulated with a ring oscillator (ROSC) circuit. Fig. 6(a) presents a ROSC with the switching capacitances of each stages are same. In contrast, the ROSC in Fig. 6(b) is comprised of a different number of inverters at each stage. This ROSC presents a canceling capacitor that is unmatched. The simulation results are plotted in Fig. 6(c). The substrate contact space is 160 μ m. Compared with the substrate noise generated by four switching inverters in Fig.5(a), the substrate noise of Fig. 6(a) ROSC is suppressed by about 30%. Even with Fig. 6(b), which has an uneven number of canceling inverters, the substrate noise is suppressed by about 50%. These results indicate that in a data path circuit in which some substrate noise is acceptable, more than 100 μ m of substrate contact space is allowed, and the substrate contact area overhead decreases to less than 1 %.



Fig. 5. Substrate Noise correlation with substrate contact space at each Switching mos number



Fig. 6. results of simulation opposite direction switching capacitor canceling effect $$\rm IV.$$ CHIP MEASUREMENT RESULTS

The substrate-noise infuluence is measured using a ROSC. Fig. 7 is a chip photograph. This chip was fabricated using a 65 nm process and triple

well structure. There are four modules that comprise a ROSC array, and the frequency of one ROSC was measured. The substrate contact space of the four modules were 20 μ m, 80 μ m, 160 μ m, and 320 μ m. The measurement and simulation results of ROSC frequency correlation with substrate contact space plotted in Fig. 8(a). In measurement of each process corner, there is less than 2% difference on each substrate contact space. The differences in th simulation results are smaller than 0.5% on each substrate contact spaces.

Fig. 8(b) shows the correlation of ROSC cycle delay with bias between the source and the substrate. From Fig. 8 and Fig. 6, we estimate that the fluctuation in the transistor switching speed is less than 3% at the data path. Therefore, in regions where we can expect noise canceling transistor switching conditions, we can reduce the circuit area by spreading the substrate contact space. With a substrate contact space of 100 μ m, the data path area overhead with substrate contact is reduced to less than 0.6% accepting 3% fluctuation in transistor switching speed.



Fig. 7. Photograph of test chip. 65 nm, LP, Triple Well



Fig. 8. Measurement results of Ring Oscillator frequency correlation substrate contact space and Transistor switching speed shift with bias between source and substrate

V. CONCLUSION

To optimize space of substrate contacts, substrate noise characteristic of digital circuits is analyzed with 65nm process. well-RC model considering well device structure is important to improve estimation accuracy of substrate noise. There is $30 \sim 50\%$ difference with conventional model. The area substrate contact suppressing substrate noise is limited about 13 μ m. The affect of transistor switching timing and voltage is large. If 16 inverters switches same time as big buffer MOS, about 200 mV substrate noise is generated. Such circuits needs approximate substrate contact. But it is possible to reduce substrate contacts at circuits expected substrate noise canceling like data path. Therefore if 3% transistor switching speed fluctuation is accepted, then data path area is reduced about 10% with 100 μ m space of substrate contact. And it is measured that Ring Oscillator frequency shift with substrate contact space is smaller than 2%.

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REFERENCES

- [1] David K. Su, et. al., 1993 IEEE JSSC, vol.28, pp. 420-430.
- [2] Emre Salman, et. al., 2008 IEEE ISQED, pp.261-266.
- [3] Makoto Nagata, et. al., 2002 IEEE ASP-DAC, pp.71-76.
- [4] J. Briaire, et. al., 2000 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.19, pp.645-653.
- [5] Makoto Nagata, et. al., 2001 IEEE JSSC, vol.36, pp. 539-548.
- [6] Mustafa Badaroglu, et. al., 2006 IEEE Transactions on Circuits and Systems, vol.53, pp.296-305.