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Within-Die/Wafer Variation Analysis of Basic CMOS Circuits Based on Surface-Potential-Model HiSIM2

Koh Johguchi[1], Akihiro Kaya[2], Shinya Izumi[2], Hans Jürgen Mattausch[2,3], Tetsushi Koide[2,3] and Norio Sadachika[1,2]

[1]HiSIM Research Center, Hiroshima University, 1-3-1 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8530, Japan
[2]Graduate School of Advanced Sciences of Matter, Hiroshima University
[3] Research Institute for Nanodevice and Bio Systems, Hiroshima University

1. Introduction

The scaling down of MOSFET has enhanced VLSI performance. On the other hand, process variations become also remarkable due to the miniaturization. Process variations may therefore increasingly degrade reliability and yield of VLSI circuits due to unexpected changes of MOSFET. Consequently, it is important to construct a design method which allows the reliable design of circuits having robustness in their functionality even under enhanced process variations.

Here, we report a process variation analysis based on the surface potential MOSFET model HiSIM2 [1]. Ring oscillators, amplifier stages with feed-back coupling [2] and SRAM cells, which fabricated at the 180-nm technology nodes, are used for the variation analysis as examples of basic circuit elements.

2. MOSFET-Variation Extraction with HiSIM2

The HiSIM2 model is one of the next generation MOSFET models for SPICE simulations, based on the complete drift-diffusion theory. Process-variation sources can be unambiguously correlated to specific microscopic model parameters of HiSIM2. Moreover, corner variation models for circuit simulation can be realized changing only four most sensitive parameters, namely, *NSUBC*, *MUESR1*, *NSUBP* and *XLD* (Table I).

From the measurement results of single MOSFETs in 180-nm CMOS technology, the within-wafer variations have been determined (see Table II) and are verified to reproduce the drain saturation current (I_{on}) and threshold voltage (V_{th}) variation for all gate-length (L) [3]. In the following sections, these MOSFET-parameter variations are used for the variation analysis of basic CMOS circuits.

3. Variation Analysis of Basic CMOS circuits

3.1 Amplifier Stage with Feed-Back Coupling

The schematic diagram of an amplifier stage with feed-back coupling (FBC) is shown in Fig. 1. Due to the construction with only one transistor type, NMOS or PMOS variations can be examined independently. FBC can also separate within-die and within-wafer variations with the hysteresis property of its output characteristic for appropriately designed transistor sizes [2]. The hysteresis shift (H_{sh}) is directly corresponding to within-wafer variations, while the hysteresis width (H_w) is caused by within-die (local) variations. Figure 2 gives the H_{sh} and H_w variation measurements of NMOS-type FBCs in the 180-nm CMOS technology for short and long gates. Table III verifies the reproducibility of within-wafer variation extraction with HiSIM2 in comparison to single MOSFET results and the additional possibility of local within-die variation extraction. Although the *NSUBC* within-wafer variation from the FBC result is slightly larger than that from single NMOS transistors, the variation results are very well reproduced with the 4 key parameters of HiSIM2.

3.2 Ring Oscillators

Ring oscillators have an odd number of inverter stages which are connected into a ring. Due to their simple composition, ring oscillators are often used to analyze the effects of transistor variations on basic circuits. Figure 3 shows the measured oscillation frequency variations of a 180-nm CMOS technology including their power supply voltage dependence. Within-wafer variation from die-to-die is a global variation which affects all transistors of the circuit in the same way, while within-die variation is largely random variation, which affects each transistor of the circuit differently. Therefore, within-die and within-wafer variations can be separated with ring oscillators because the random variations are increasingly averaged with large number of transistors [4]. From Fig. 3, it can be seen that the within-die variation is approximately exponentially increasing for lower supply voltage, although the within-wafer variation increases only proportionally to the inverse of the supply voltage.

As well as FBC analysis, the reproducibility of the within-wafer/die variations is verified by fitting HiSIM2 parameters to the ring oscillator measurement results (see lower half parts of Table III). The extracted parameters show much the same pattern compared to the FBC results. Deviations can be observed for the within-die variation, which may be due to larger special separation of the transistors in the ring oscillator.

3.3 Static Random Access Memories (SRAM)

SRAM is a basic element of logic circuits and occupies the largest area in recent VLSI circuits. Hence, SRAM sensitivity to process variations is very critical and providing a large static noise margin (SNM) of SRAM-cells becomes a very serious problem. For improvement of the SNM, the channel width of the driver transistors (W_{dr}) is often set to a lager value than that of transfer transistors (W_{tr}) in the 6-transistor SRAM cell (6Tr-cell), as shown in Fig. 4. However, increasing of the β-ratio, which is defined by $\beta = W_{dr}/W_{tr}$, can cause larger SNM variations due to an abrupt widening bump of the diffusion in the SRAM cell layout. Figure 5 shows the β-ratio dependence of the measured SNM and I_{on} variations of each transistor in 180-nm CMOS technology. From Fig. 5a, the SNM of the 6Tr-cell and its variation is improved as the β-ratio is increased. I_{on} variations of load and transfer transistors, however, have been degraded, although the I_{on} variation of the driver transistor is decreased (Fig. 5b), as expected from the larger driver-transistor size. The reproducibility of the measured SNM variations with HiSIM2 is verified in Fig. 6, by using the microscopic HiSIM2-parameter variation result of the FBC analysis.

4. Conclusions

A variation analysis based on the HiSIM2 surface-potential model has been presented for basic circuits in the 180-nm CMOS technology. Only four microscopic parameters, *NSUBC*, *MUESR1*, *NSUBP* and *XLD*, are sufficient for reproduction of within-wafer and within-die variations. With ring oscillators and FBC circuits, these within-wafer and within-die variations can be separated. To analyze the layout dependency of 6Tr-SRAM-cells, SNM and I_{on} variations have been measured in the 180-nm CMOS technology. SPICE simulations based on HiSIM2

are in good consistency with the measured variations of all test circuits.

Acknowledgements

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Table I The most sensitive 4 parameters of HiSIM2 for the realization of process variations.

Parameter	Meaning
NSUBC	Substrate doping concentration
MUESR1	Mobility degradation due to gate-oxide roughness
NSUBP	Peak pocket doping concentration
XLD	Channel-length change

Table III Extraction results of MOSFET variation boundaries for the HiSIM2 parameters from measured FBC and ring oscillators (RO) in the 180-nm CMOS technology.

TEG	MOS type	Variation type	*NSUBC* [%]	*MUESR1* [%]	*NSUBP* [%]	*XLD* [nm]
FBC	PMOS	Within-wafer	-4.2/+4.0	+/- 0	-2.3/+2.1	-4.5/+5.0
		Within-die	+/- 0.8	+/- 0	+/- 0.6	+/- 1.0
	NMOS	Within-wafer	-3.4/+3.3	-9.7/+10	-1.6/+1.5	-4.7/+5.5
		Within-die	+/- 1.2	+/- 0	+/- 1.0	+/- 2.5
RO	PMOS	Within-wafer	-7.5/+7.3	+/- 0	-2.6/+2.6	-4.8/+4.4
		Within-die	-2.0/+1.7	+/- 0	-4.2/+1.5	-3.1/+1.3
	NMOS	Within-wafer	-2.7/+2.8	-9.7/+10	+/- 2.1	-8.0/+7.7
		Within-die	-1.9/+1.7	+/- 0	-0.5/+0.9	-1.8/+1.3

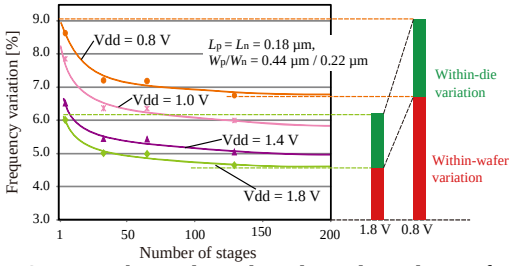
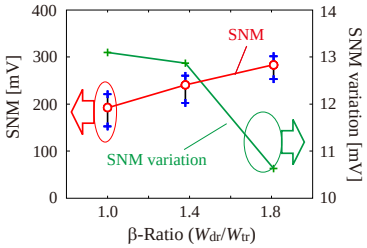
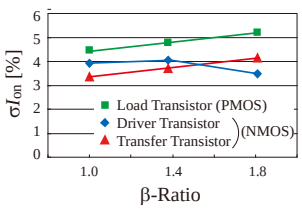


Fig. 3 Stage number and supply-voltage dependence of measured ring-oscillator frequency in the 180-nm CMOS technology. Frequency variations are normalized by the average of the measured oscillation frequency. The effects of within-wafer and within-die variations can be separated with these ring oscillator measurements as indicated on the right side of the graph.



(a) β-ratio dependence of static-noise margin (SNM) and its variation.



(b) Variations of drain saturation current (I_{on}).

Fig. 5 Layout dependency of measured SNM and I_{on} variations in a 6Tr-SRAM cell .

References

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Table II MOSFET variation boundaries from the nominal parameter set for the most sensitive HiSIM2 parameters in the 180-nm CMOS technologies.

MOS-type	*NSUBC* [%]	*MUESR1* [%]	*NSUBP* [%]	*XLD* [nm]
PMOS	-5.4/+9.5	+/- 0.0	-2.9/+2.2	-4.5/+5.0
NMOS	-2.9/+2.7	-9.7/+10	-2.2/+2.0	-7.0/+9.0

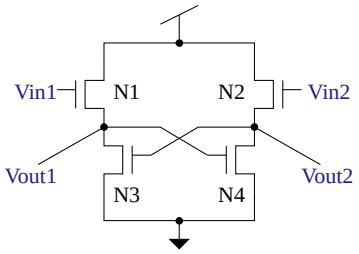
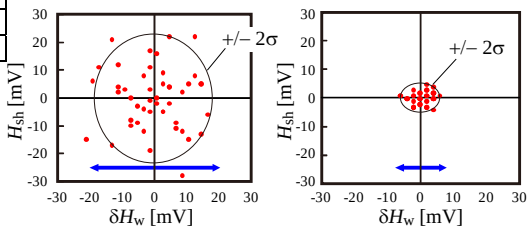


Fig. 1 Schematic diagram of an amplifier stage with feedback coupling (FBC) constructed from NMOS transistors.



(b) L = 0.18 µm (b) L = 2.0 µm

Fig. 2 Hysteresis shift (H_{sh}) and width (H_w) variation from the measurement of NMOS FBC circuits. Due to only 52 samples, 2σ circle is drawn in the graph. The arrow of horizontal direction represents simulated the within-wafer variation from extracted data of single NMOSFET (Table II).

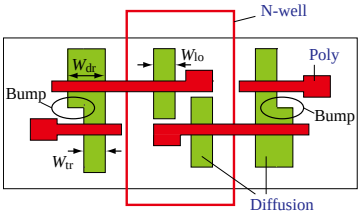


Fig. 4 Layout of the 6Tr-SRAM cell. Bumps of NMOS diffusion are generated by designing for an increased β-ratio.

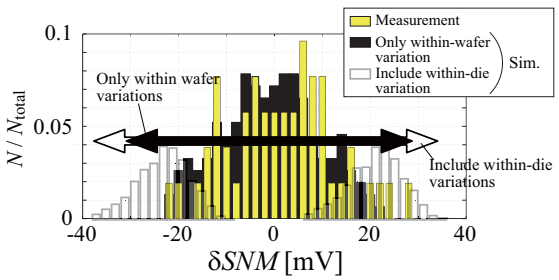


Fig. 6 SNM-variation reproduction with the HiSIM2 parameter set of Table II. Including within-die variations, the measurement data is in good agreement with the HiSIM2 simulation.