Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1076-1077

D-8-1(Invited)

Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects

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Abstract

This paper provides an overview of the state-of-the-art of 1-D carbon nanomaterials with regard to their applicability in ICs as interconnects (including through-Si vias) and passive elements, as well as off-chip components.

1. Introduction

Low-dimensional allotropes of carbon, known as carbon nanomaterials, have extraordinary physical properties. Particularly the 1-D forms, carbon nanotubes (CNTs) and graphene nano-ribbons (GNRs), have been extensively investigated for their exciting prospects in a variety of applications including VLSI [1]. A summary of the key properties of carbon nanomaterials is provided in **Table I**. All of these unique properties indicate that CNTs and GNRs could be potentially employed as alternative materials for next-generation IC interconnects and other applications.

2. Fabrication and Integration

For CNT interconnect applications, chemical vapor deposition (CVD) methods are most suited due to the ability of selective growth, large area deposition, and aligned CNT growth. For CNT vias, both conventional etch first or "Top-down" approach [2] as well as "Bottom-up" approach [3] have been pursued. Most recently, low temperature (365^{o}C) growth and fully integrated on-chip CNT vias with Cu and ultra low-K (ULK) dielectric have been achieved [2]. However, still quite a few challenges remain, such as, growing dense bundles of CNTs (especially the single-walled form); controlling chirality to ensure that the CNTs (in case of single-walled) forming a bundle are all metallic; growing long horizontal CNT bundles [1]; to name a few.

GNRs are believed to be more controllable than the CNTs due to their apparent ease of fabrication by patterning graphene. However, while various methods of fabricating graphene, such as mechanical exfoliation and thermal decomposition of single crystal SiC, have been pursued, but they are difficult to be integrated into the VLSI backend process. On the other hand, method of fabricating graphene first and then transferring to a desired substrate has been proposed [4]. While this approach still requires further investigation, they are more suitable for interconnect related applications [5]. Most recently, Fujitsu has demonstrated the possibility of building "all carbon" interconnect structures by combining CNTs (as via) and GNRs (as horizontal wire) [6].

3. Interconnect Application

Resistance: The conductance of CNT/GNRs can be derived using the linear response Landauer formula as shown in detail in [1]. From the resistance comparison (**Fig. 1**), it can be observed that for all types of CNTs and GNRs, their resistances decrease with increasing length and become stable after 10 μm. For longer lengths, all types of CNTs could offer lower resistance than Cu, whereas, only AsF_5 intercalation doped multi-layered GNRs with high specularity can provide lower resistance than that of Cu.

Delay: The *RLC* equivalent circuit models have been proposed in [7][8] for CNTs and in [5] for GNRs, as shown in **Fig. 2**. **Fig. 3** shows the delay ratios of CNT and GNR interconnects with respect to Cu at the global level. It is shown that most CNTs outperform Cu, while doped GNR with p= 0.41 is worse than Cu. Ideal case multi-layer GNR (doped and p=1) can outperform Cu but still cannot be better than ideal case CNT. **Fig. 4** shows that the performance of CNT/GNR interconnects are comparable with that of Cu except for monolayer or diffusive GNRs.

High-Frequency: Due to the existence of large kinetic inductance, the high-frequency effect in CNT bundle is quite different from conventional metals [8]. It can be observed from **Fig. 5(a)** that the skin depths of CNTs saturate at high frequencies. **Fig. 5(b)** shows that the high-frequency resistance of CNT interconnects saturates at high frequencies. Particularly, MWCNTs exhibit a small increase in resistance with frequency.

4. Passives, TSVs, and Off-Chip Applications

Inductor: To take advantage of the unique high-frequency properties of CNTs, CNT based on-chip inductors have been designed and analyzed [9]. **Fig. 6(a)** shows that the direct impact of the large kinetic inductance of CNTs on the Q factor is negligible [8]. However, it can be observed that for a low-loss substrate (**Fig. 6(b)**), the maximum Q factor of a 0.75 turn inductor can be increased by as much as 230 % (3.3 times) by replacing Cu with CNTs. This significant enhancement in Q factor arises not only because of the lower *d.c.* resistance of CNTs, but also because of the reduced skin effect in CNT interconnects as discussed above.

Capacitor: Small form factors and high surface-area-to-volume ratio of CNTs is very desirable for capacitor applications. Simulation results shown in [1] indicate that the capacitance density of CNT based capacitors (shown in **Fig. 7(a)**) can reach 38.39 fF/μm^2, much larger than the ITRS requirement of 12fF/μm^2 for year 2022.

Through-Silicon Vias: CNT bundles can potentially offer excellent electrical and thermal properties, making them excellent candidates for TSVs in 3-D ICs. Well aligned high aspect-ratio CNT bundles have been fabricated and CNT based TSVs have been demonstrated in [10] (**Fig. 7(b)**).

Off-Chip Applications: Besides on-chip interconnect related applications, CNTs can also be used as chip-to-packaging interconnects. Utilizing CNTs as flip-chip bumps for the packaging of high power amplifiers (HPA) has been demonstrated in [11] (**Fig. 8(a)**) and has shown that CNT bumps can enhance the HPA high-frequency performance and facilitate heat removal. Recently, patterned CNTs have been used as heat spreader for chip cooling (**Fig. 8(b)**) [12], which not only achieves better thermal performance compared to Cu cooling structure but also provides light-weight and mechanically-stiff cooling system.

5. Conclusions

CNT based interconnects could provide better delay performance than that of Cu for long lengths. However, it has been shown that in order for GNR interconnects to be comparable to CNTs and Cu interconnects, intercalation doped multilayer GNRs with high edge-specularity are needed. High-frequency analysis of CNT interconnects reveals that skin effect is significantly reduced in CNT bundles and, as a result, CNT based inductors could offer more than 3X quality factor enhancement over Cu based inductors. Other applications of CNTs, such as high-density capacitors, high aspect-ratio TSVs in 3-D ICs, and chip-to-packaging interconnects also offer exciting prospects.

References

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Table I. Properties of Carbon Nanomaterials Relevant to VLSI Interconnects and Passives [1]

	Cu	SWCNT	MWCNT	Graphene or GNR
Max current density (A/cm^2)	10^7	$>10^9$	$>10^9$	$>10^8$
Melting point (K)	1356	3800 (graphite)		
Thermal conductivity ($\times 10^3$ W/mK)	0.385	1.75-5.8	3	3-5
Mean free path (nm) @ 300K	40	$>10^3$	2.5×10^4	1×10^3

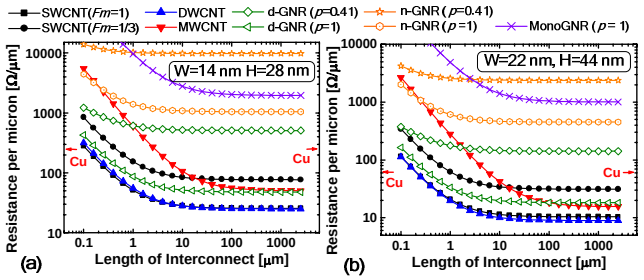

Fig. 1. Resistance per unit length comparison for different types of CNT and GNR interconnects. For DWCNT, the diameter is set to be 1.5 nm, metallic fraction *Fm*=1. The diameter of MWCNT and the width of GNR are set to be equal to the wire width (*W*). n-GNR and d-GNR represent neutral multilayer GNRs and AsF_5 intercalation doped multilayer GNRs, respectively. *p* is the edge specularity.

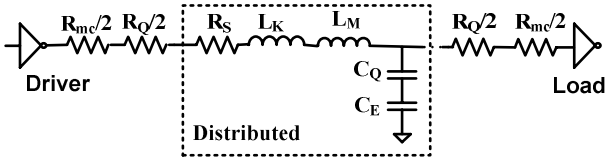

Fig. 2. The equivalent distributed circuit model of an SWCNT or GNR interconnect. R_{mc} is the imperfect contact resistance, R_Q is the quantum contact resistance, R_S is the scattering induced resistance, L_K and L_M are the kinetic inductance and magnetic inductance of the shell, respectively. C_Q and C_E are the quantum capacitance and electrostatic capacitance, respectively.

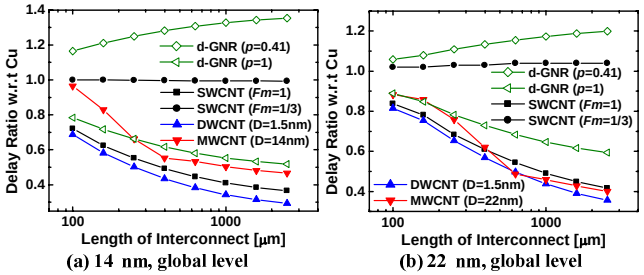

Fig. 3. Signal delay ratios (with respect to Cu) of SWCNT, DWCNT, MWCNT and different types of GNRs at global level for (a)14 nm, (b) 22 nm, technology node. *Fm* indicates the fraction of metallic SWCNTs in the SWCNT bundle; *p* indicates the specularity of GNR edge. d-GNR represent AsF_5 intercalation doped GNRs.

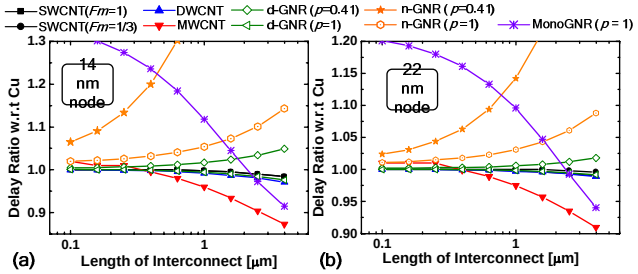

Fig. 4. Signal delay ratios (with respect to Cu) of SWCNT, DWCNT, MWCNT and different types of GNRs at local interconnect level for (a) 14 nm, (b) 22 nm, technology node. *Fm* indicates the fraction of metallic SWCNTs in the SWCNT bundle; *p* indicates the specularity of GNR edge; n-GNR and d-GNR represent neutral multilayer GNRs and AsF_5 intercalation doped multilayer GNRs, respectively.

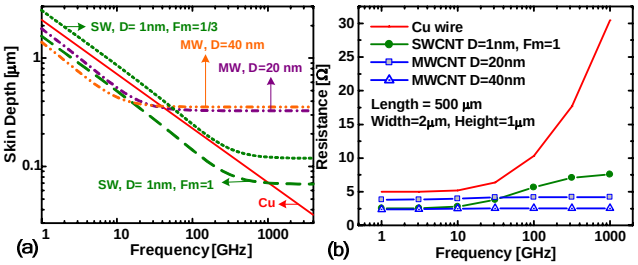

Fig. 5. (a) Skin depth of different types of CNT materials as well as Cu as a function of frequency. (b) High-frequency resistance of CNT and Cu.

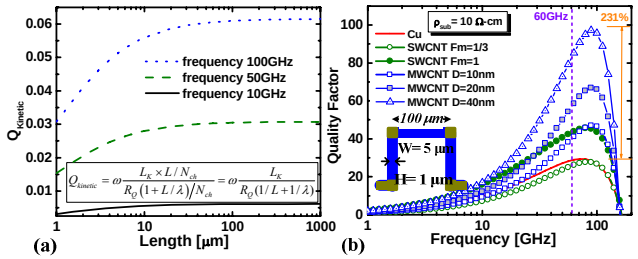

Fig. 6. (a)The Q factor due to kinetic inductance, $Q_{kinetic}$, as a function of frequency and length. The equation used for calculating $Q_{kinetic}$ is shown in the inset. λ is assumed to be 1 μm.(b) Quality factor of 0.75 turn inductors based on Cu, SWNCT, and MWCNT interconnects as a function of frequency for substrate resistivity ρ = 10 Ω·cm (low loss).

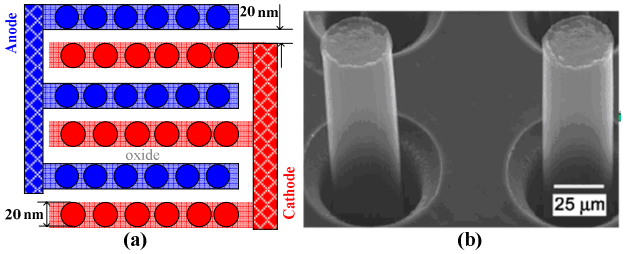

Fig. 7. (a) One feasible vertical high aspect-ratio CNT capacitor structure. Red color CNTs are cathode, while blue color CNTs represent anode. The CNTs are assumed to be MWCNT with diameter = 20 nm. (b) Two fabricated CNT bundles as through-silicon vias [10].

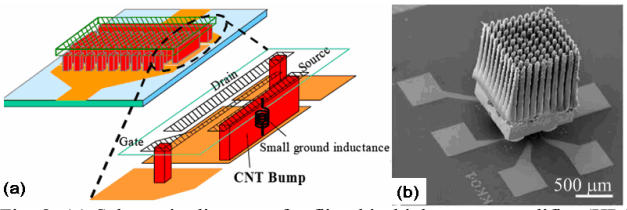

Fig. 8. (a) Schematic diagram of a flip-chip high power amplifier (HPA) packaging employing CNT bumps, which provide thermal conductivity as high as 1400 W/m-K. [11], (b) SEM image of an assembled CNT heat spreader [12].