Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1094-1095

Integration and dielectric reliability of 30nm ½ pitch structures in Aurora®LK HM

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Abstract

Aurora®LK HM (k=3.2) material has been successfully integrated in 30nm ½ pitch structures. This material outperforms Aurora®LK (k=3.0) in terms of breakdown field strength and mechanical properties. Scaling of PVD based barrier/seed process and fine-tuning of the barrier CMP overpolish condition were yield enabling. No degradation of the breakdown field is observed at 30nm ½ pitch for line lengths up to at least 1mm. The median TDDB lifetime, evaluated on a 70nm pitch structure, exceeds 10 years at an electrical field of 0.7MV/cm.

Introduction

The ITRS roadmap predicts scaling towards 30nm DRAM contacted ½ pitch by 2013-2014 [1]. At the same time high operating voltages in memory devices call for sufficient current carrying capacity of the Cu lines which can be achieved by increasing the aspect ratio (AR) of the damascene lines. In this paper we report on the integration and dielectric reliability of a k=3.2 material into 30nm ½ pitch damascene structures of AR=4.

Aurora®LK and Aurora®LK HM intrinsic properties

For integration two materials were considered: Aurora®LK and Aurora®LK HM. Both can be deposited in the same chamber on an ASM® Eagle12® platform. Their mechanical properties were evaluated by nano-indention. K-value and intrinsic dielectric breakdown field were evaluated on planar capacitors as a function of thickness. Higher mechanical strength and resistance to dielectric breakdown were found for the LK HM material with only a small penalty in terms of k value (Table 1). This makes the material particularly suitable for integration into high AR and narrowly spaced structures.

Integration into 30nm ½ pitch structures

The stack consisted of 5nm SiCN/25nm SiCO liner + 120nm Aurora®LK. In case of Aurora®LK HM, the top 30nm low-k was replaced by partially sacrificial PECVD SiO_2 to increase etch rate, and to reduce the possible damaging impact of ash, Cu oxide reduction plasmas and CMP (Fig. 1).

We adopted a double patterning scheme using 30nm TiN metal hard mask (MHM) as described in Fig. 1 similar to the scheme used earlier for 50nm ½ pitch integration [2]. Each time resist lines of 60nm at a minimum pitch of 120nm were patterned using immersion lithography on a ASML1900i scanner. These were transferred as 30nm trenches into TiN MHM using Cl-based etch chemistry for BARC/TiN opening in combination with a Motif® shrink process. An O_2/Cl_2 based ash was used to remove remaining BARC/resist. This step was followed by a short diluted HF (dHF) wet clean to prevent hard mask corrosion. Transferring the double pattern at 60nm minimal pitch into the low-k stack was done in a Flex45 Exelan® etch chamber using $Ar/CF_4/O_2$ chemistry for LK HM + SiO_2 and $Ar/N_2/CO/C_4F_8/O_2$ for LK [3]. Again this step was complemented with dHF clean step and a dedicated post etch residue removal step (PERR) for which inorganic and solvent based cleans were compared.

Polymer residue was found to be quite abundant on the LK test wafers as compared to LK HM, which is attributed to the more polymerizing nature of the etch chemistry used for LK (Fig. 2). As a result, impact of the PERR scheme chosen on the electrical performance of narrow metal lines is small for LK HM, while substantial differences are observed on LK with the best result obtained for dHF combined with a solvent based clean step. However, regardless of the PERR scheme evaluated, we could still identify remaining residue on large dummy features. In case dHF was part of the sequence, the residue could be partially detached from the sidewall but it was not dissolved.

Fig. 3 shows TDSEM and X-TEM images after metallization indicating that integration is challenged by a substantial loss of dielectric spacing. This results into shorts on meander-fork test structures at 60nm (1:1) pitch. A mild overpolish at CMP is sufficient to increase yield significantly on the LK HM stack wafers (Fig. 4). Removal of etch induced damage on the narrow low-k spacing sideall by the PERR process, revealing the MHM undercut after CMP could be excluded as root cause based on XTEM images after electroplating (Fig. 3 right). The CD widening at trench top is being investigated and could result from MHM erosion during etch (notice the MHM is virtually absent on Cu-filled structures before CMP), the presence of uncleaned sidewall polymer or an unoptimized CD measurement algorithm.

EFTEM maps on the LK HM stack indicate partially intact oxide hard mask after CMP (Fig. 5). Some carbon depletion is observed in the top 15nm of LK HM which is attributed to the use non-diluted NH_3 Cu reduction plasma and the cap oxide deposition. However overall similar carbon content is observed in patterned and unpatterned regions, indicating little patterning induced low k damage.

For metallization we compared the unscaled barrier/seed sequence, previously used for 50nm ½ pitch integration (process A), and scaled versions of the PVD based TaN/Ta barrier and Cu seed processes optimized for reduced risk for pinch off at trench top (process B). There is an obvious positive impact of the overall filling quality and a reduction in the fraction of dies with elevated sheet resistance (voids) moving to process B (Fig. 6 and 7).

Dielectric reliability of 30nm ½ pitch structures

The breakdown field (E_{BD}) was evaluated on short and long parallel lines (PL) and meander-forks (MF) with top dielectric spacing of 16nm and 26nm corresponding to 60nm (1:1) and 70nm pitch (1:1.25) test structures. Benchmarking the obtained values to what was obtained earlier at 50nm spacing [2] and on intrinsic material (Table 1) comparable E_{BD} values down to 16nm for PL with limited length are obtained (Fig. 8). Larger line lengths and turnings in the layout reduce E_{BD}, linked to higher statistical probability of local field enhancement due to marginal spacing induced by inadequate OPC or line edge roughness.

TDDB measurements were performed on a 70nm pitch (1:1.25) 1mm PL. The dataset obtained on 3 voltage conditions was fit adequately using a lognormal distribution (Fig. 9). The median lifetime of 10 years is deduced to be reached at a field of 0.7MV/cm assuming an E-model based extrapolation.

Conclusions

30nm ½ pitch AR=4 structures were successfully integrated into Aurora LK HM. The feasibility to fabricate structures with similar E_{BD} at 16nm as compared to 50nm spacing was demonstrated indicating the potential of the Aurora®LK HM for use in advanced memory devices.

Table 1: Comparison of intrinsic material properties of LK and LK HM.

Material	E (GPa) H (GPa)	k	E_{BD} (MV/cm) 20nm	E_{BD} (MV/cm) 40nm	E_{BD} (MV/cm) 60nm
Aurora® LK	12.3 1.2	3.1 ± 0.1	5.7 ± 0.4	9.7 ± 0.4	9.5 ± 0.2
Aurora® LK HM	16.8 1.8	3.2 ± 0.1	7.3 ± 0.6	10.5± 0.4	11.0 ± 0.3

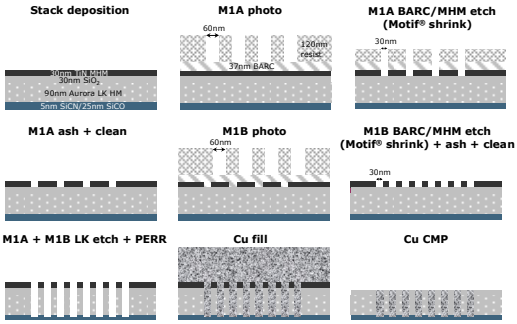

Fig. 1: Description of the double patterning processing sequence to obtain 30nm ½ pitch structures in LK or LK HM.

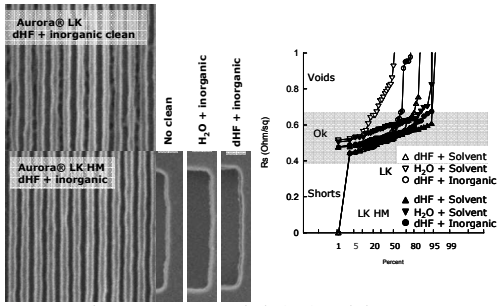

Fig 2: TDSEM images on 60nm pitch (1:1) and dummy square structures after etch and clean (left). Sheet resistance of off-pitch 30nm trenches for various clean options for both LK and LK HM.

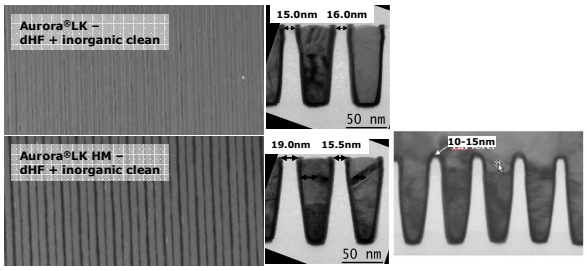

Fig. 3: TDSEM and XTEM images after metallization and CMP for LK and LK HM. The XTEM image on the right after electroplating indicates virtual absence of TiN MHM before CMP.

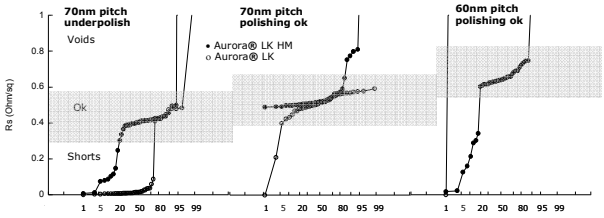

Fig. 4: Impact of a CMP overpolish tuning on the meander sheet resistance and electrical yield of 70nm (1:1.25) and 60nm (1:1) pitch structures for LK and LK HM.

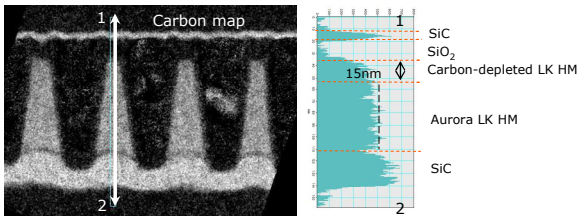

Fig. 5: EFTEM image of the carbon presence in the integrated LK HM stack (left) and top to bottom evaluation of the carbon signal strength in the narrow spacing.

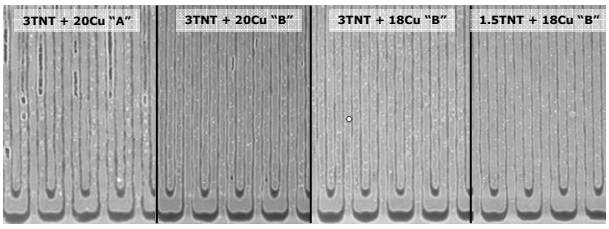

Fig. 6: TDSEM images on LK HM after metallization and CMP for the indicated thickness of TaN/Ta (TNT) barrier and Cu seed for process variant A and B, the latter being tuned for reduced pinch off at the trench top.

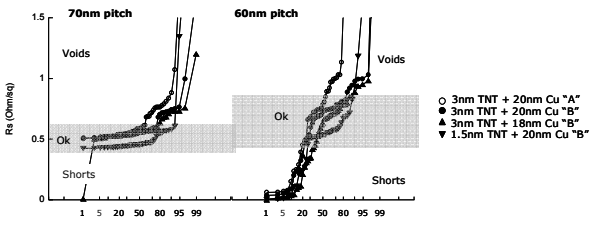

Fig. 7: Impact of the barrier/seed process choices on the meander sheet resistance and yield for 70nm (1:1.25) and 60nm (1:1) pitch meander forks in LK HM.

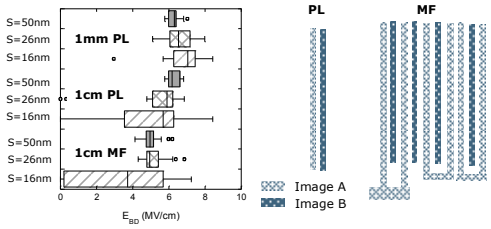

Fig. 8 E_{BD} scaling vs spacing as a function of test structure layout.

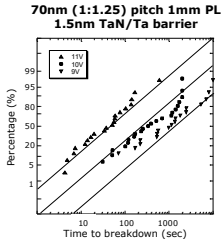

Fig. 9 Lognormal fit of time-to-breakdown data for 3 experimental conditions on a 70nm pitch (1:1.25) 1mm PL structure.

References

[1] ITRS roadmap

[2] S. Demuynck et al., JJAP Vol. 48(4), 04C018

[3] C. Huffman et al., MAM2009 Proc. (accepted)