Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp806-807

E-3-1L

A Compact Space and Efficient Drain Current Design for Multi-Pillar Vertical MOSFET's

Koji Sakui and Tetsuo Endoh
Center for Interdisciplinary Research, Tohoku University, JST-CREST
Aramaki aza Aoba 6-3, Aoba-ku, Sendai, 980-8578, Japan
Tel: +81-22-795-5260, Fax: +81-22-795-7810, Email: koji.sakui@cir.tohoku.ac.jp

Introduction: Recent studies focused on the vertical MOSFET's have brought out their performance merits, such as 1) the transistor area reduction for the circuit design, 2) no threshold increase by the back-bias effect, 3) the suppression of the short channel effect, 4) the sub-threshold swing decrease, and 5) the increase in the current density [1]-[3].And also, its multi-pillar vertical MOSFET characteristics have been studied [2]-[3]. However, due to the device structure of the vertical MOSFET, the bottom of its silicon pillar has a certain resistance because there is a diffused silicon wiring area in the bottom. Thereby, this resistance becomes large in the case of the multi-pillar transistors and also shows the asymmetric characteristics between the top and bottom nodes of the pillar. This paper is devoted to examining this resistance for the multi-pillar vertical MOSFET and proposing the compact design, which can suppress the resistance influences and attain a large drain current.

Features of vertical MOSFET's: Fig.1 illustrates the device structure of the vertical MOSFET's. The vertical MOSFET arranges a source, gate, and drain, which make up the silicon pillar vertically. The gate electrode surrounds the silicon pillar and the channel is separated from the substrate by the *n+* region. With its distinct device structure and layout, the vertical MOSFET's enable a higher performance than the conventional planar MOSFET's. However, the bottom *n+* region contains the certain resistance to its contact so that this resistor asymmetrically influences on the V_D-I_D characteristics whether the bottom *n+* is used for the source or drain, as illustrated in Fig.2(a). Fig.2(b) simulates the asymmetric characteristics of the vertical MOSFET. Here, the transistor size of *W/L* is 0.5μm/0.18μm, the gate oxide thickness is 5nm, and the drain or source resistor of R_D or R_S is 200Ω in this case. The model parameters for the HSPICE BSIM4 simulation are extracted from the experimental data. The drain current in the case of R_S is smaller than that of R_D because the source side resistor lowers not only the effective drain-source voltage of V_D but also the effective gate-source voltage of V_G in the saturated region, which is emphasized by the multi pillars.

Multi-pillar vertical MOSFET's: Fig.3 illustrates the 5×5 multi-pillar vertical MOSFET's of *M11~M55* are aligned in a square shape. Here, the horizontal and vertical resistances between the pillars are *R*Ω, and the diagonal resistances between the pillars are $\sqrt{2}\times R\Omega$. Fig.4 shows the Drain/Source contacts patterns for the multi-pillar transistors; Side Contacts (a) and Peripheral Contacts (b). In case of Side Contacts, the pillar transistor of *M35*, which is the furthest from the Drain/Source contact, has the largest resistance, as shown in Fig.5. Figs.6 and 7 show the simulated drain currents of the pillar transistor of *M31~M35* (a), and the local drain/source node voltages of *D31~D35* (b) in both cases of ***Bottom Node Drain*** and ***Bottom Node Source***, respectively. Here, the multi-pillar transistor of *W/L* is 0.5μm/0.18μm, the diffusion resistance of *R* is defined as 200Ω, and the gate voltage of *VG* is 2V. The drain current of *M35* is smaller that of *M31* due to the *IR* drops of the bottom resistance. Peripheral Contacts in Fig.4(b) can suppress this *IR* drops influences, however, it enlarges the layout area.

Proposed multi-pillar vertical MOSFET's: Fig.8(a) has presented the proposed multi-pillar vertical MOSFET's. Here, the pillar transistors are directly replaced by the drain contacts. Fig.8(b) compares the layout area for each case; 5×5 is pillar space for 21 transistors + 4 intermediate contacts, 5×6 pillar space is for 26 transistors + 4 intermediate contacts or 25 transistors + 5 side contacts, 7×7 pillar space is for 25 transistors + 24 peripheral contacts, and 25×2 pillar space is for 25 transistors + 25 line contacts, where 25 pillar transistors are aligned in a line. Fig.9 simulates all the cases above. In case of the side contacts, the *IR* drops of the bottom resistance cannot be ignored, especially for ***Bottom Node Source*** so that its drain current is reduced by 20%. It is essential to note that the drain current of the proposed 5×6 multi-pillar vertical MOSFET's is the same as those of 7×7 and 25×2 pillar space cases, which require more than 70% larger layout area. For the symmetric characteristics of Drain and Source, and the simple process, the contacts can be allowed on the *Top Node* of the pillars. Fig.10 shows the symmetric *Top Nodes* of 15 Drain's and 15 Source's. Due to the *IR* drops by two transistor connection in series, its drain current ×2 still becomes much smaller than those of the proposed cases of 26 transistors + 4 intermediate contacts with *Bottom Node Drain* or *Source*.

Conclusion: The compact and efficient design for the multi-pillar vertical MOSFET's has been proposed. It can attain the larger drain current with the smaller layout area than that of the conventional multi-pillar vertical MOSFET's.

Acknowledgment: This work has been supported in part by a grant from "Research of Innovative Material and Process for Creation of Next-generation Electronics Devices" of CREST of the Japan Science and Technology Agency (JST).

References:

[1] T. Endoh, et al., IEICE Trans. Electron., Vol.E80-C, no.7, pp.911-917, July 1997.
[2] A. Nitayama, et al., *IEEE Trans. Electron Devices*, vol.38, no.3, pp.579-583, Mar. 1991.
[3] Y. Norifusa, et al., *IMFEDK Dig. Tech. Papers*, pp.27-28, May 2008.

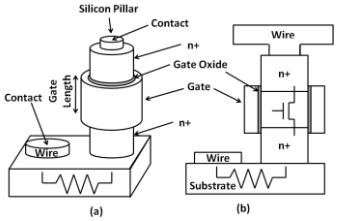
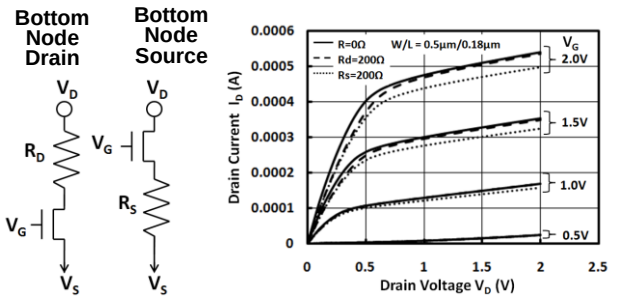
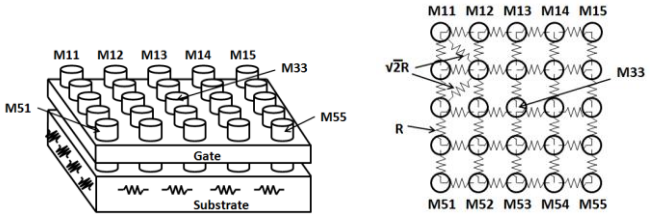


Fig. 1 Bird's eye view (a) and cross-sectional view (b) of Vertical MOSFET. The bottom n+ region contains the certain resistance to its contact so that this resistor asymmetrically influences on the device characteristics



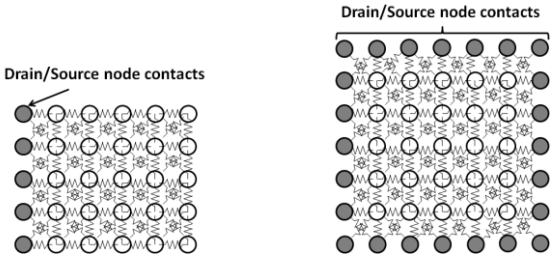
(a) (b)

Fig.2 The vertical MOSFET asymmetric characteristics. (a)Configurations whether the bottom n+ is used for the source or drain. (b)The simulated asymmetric V_D-I_D characteristics of the vertical MOSFET.



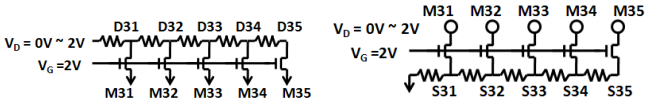
(a) (b)

Fig.3 Bird's eye view (a) and top view (b) of the 5×5 multi-pillar vertical MOSFET. There are retiform resitators in the bottom nodes of substrate. Here, the horizontal and vertical resistances between the pillars are RΩ, and the diagonal resistances between the pillars are $\sqrt{2}\times$RΩ.



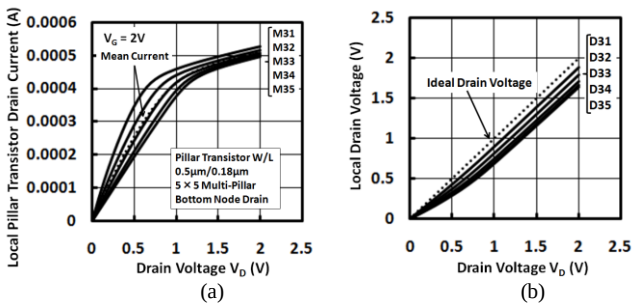
(a) Side Contacts (b) Peripheral Contacts

Fig.4 Drain/Source contacts patterns for the 5×5 multi-pillar transistors; Side Contacts (a) and Peripheral Contacts (b), where the bottom node drain is adopted.



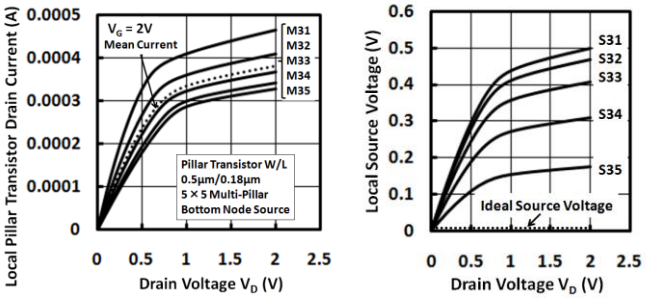
(a) Bottom Node Drain (b) Bottom Node Source

Fig.5 A part of equivalent circuit of M31-M35 in the 5×5 multi-pillar transistor array.



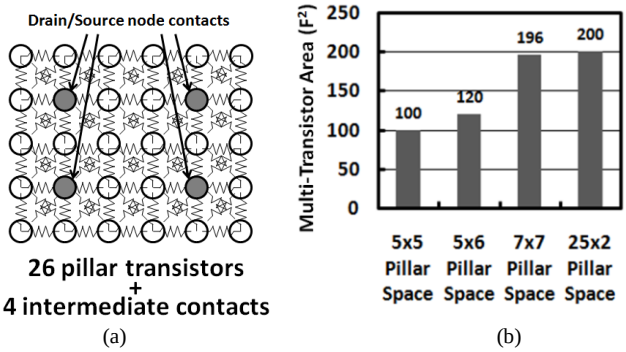
(a) (b)

Fig.6 Simulated drain currents of *M31~M35* (a), and the local drain node voltages of *D31~D35* (b) in case of ***Bottom Node Drain***.



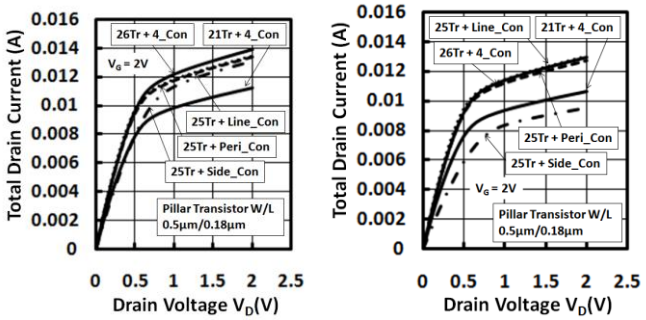
(a) (b)

Fig.7 Simulated drain currents of *M31~M35* (a), and the local source node voltages of *S31~S35* (b) in case of ***Bottom Node Source***.



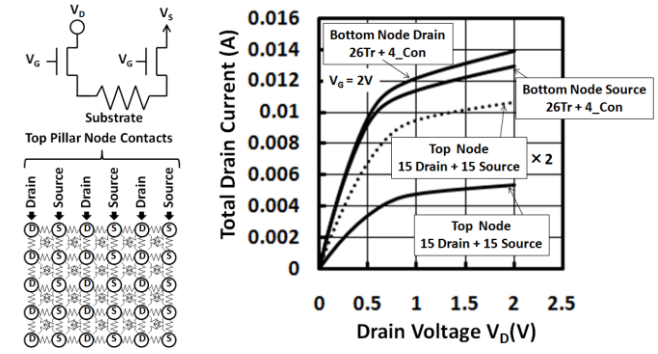
(a) (b)

Fig.8 Proposed Drain/Source contacts pattern for multi-pillar transistors (a) and Multi-pillar transistor area comparison (b). Here, 5×5 is pillar space for 21 transistors + 4 intermediate contacts, 5×6 pillar space is for 26 transistors + 4 intermediate contacts or 25 transistors + 5 side contacts, 7×7 pillar space is for 25 transistors + 24 peripheral contacts, and 25×2 pillar space is for 25 transistors + 25 line contacts, where 25 pillar transistors are aligned in a line.



(a) Bottom Node Drain (b) Bottom Node Source

Fig.9 Simulated drain current comparison. The drain current of the proposed 5×6 multi-pillar vertical MOSFET's is the same as those of 7×7 and 25×2 pillar space cases, which require more than 70% larger layout area.



(a) Top Node 15 Drain + 15 Source (b) Simulated drain current comparison

Fig.10 Symmetric Top Node Contacts of 15 Drain's and 15 Source's.