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Variability-Tolerant CMOS Gates Using Functional MOSFETs with Resistive Switching Devices

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1. Introduction

In sub-100nm CMOS technologies, variability of characteristics in individual MOSFETs causes not only performance degradation of CMOS circuits but also their assured operation. Therefore, variability compensation technique would play an important role for future CMOS technologies. Body bias technique is expected to be a promising technique for unit of functional modules of CMOS circuits [1]. Nevertheless, variability compensation for individual MOSFETs is also alternative scheme for assuring circuit operations, which would be applicable to bistable circuits such as SRAM and flip-flop.

In this paper, we present functional MOSFET (F-MOSFET) architecture using nonpolar-type resistive switching devices (RSDs) for variability-tolerant CMOS (VT-CMOS) gates. The architecture can be achieved by connecting a RSD to the source terminal of an ordinary MOSFET. The current drivability of the F-MOSFET can be modified by the resistance state of the connected RSD, which is a very useful function for variability compensation. Variability-tolerant SRAM (VT-SRAM) can be easily configured with VT-CMOSs. Using our developed SPICE macromodel for nonpolar-type RSDs, the circuit operation of the proposed VT-CMOS gates was computationally analyzed.

2. Simulation model

In our study, recently reported NiO-based RSDs [2] was used. NiO-based RSDs show very unique and useful features. In particular, the set-state resistance (R_{set}) can be controlled by a compliance current (I_{comp}) exerted during the set operation [2], that is the most important functionality for tuning of variability of MOSFET characteristics. We developed a SPICE macromodel of the RSD, and confirmed its validity, using an ordinary resistive RAM (ReRAM) cell configuration [2], as shown in Figs.1 and 2. Device parameters used for our calculation are chosen in accordance with the experimental results of Ref. [2]. The SPICE parameters were for 90nm CMOS process technology [3].

3. Functional MOSFET architecture

F-MOSFET can be easily configured by connecting a RSD to the source terminal of an ordinary MOSFET, as shown in Fig.3(a). The resistance value of the RSD can be controlled by the set operation (see Fig.2). The source-connected RSD feeds back its voltage drop to the gate and thus can vary the effective gate-source voltage (V_{GS0}). The body-source voltage (V_{BS0}) can be also modified by the resistance state of the RSD. Therefore, the F-MOSFET can exhibit variable current drivability that can be tuned by the resistance state of the RSD. Fig.3(b) shows the calculated output (I_D-V_D) characteristics of an F-MOSFET. The first quadrant shows the output characteristics in the cases of two different set-state resistances. The F-MOSFET exhibits clear transistor behavior with the different current drivabilities that depends on the set-state resistance values of the RSD. The third quadrant shows the set and reset operations for the F-MOSFET, in which V_D is grounded and V_S is pulled up, i.e., the same as the bias direction shown in Fig.1(a). In the set operation, the compliance current can be restricted by V_G. On the other hand, a high V_G value is required for the reset operation.

4. Variability-Tolerant CMOS Gates

Fig.4 shows a VT-CMOS inverter gate using an F-MOSFET (that consists of M_2 and R_n in Fig.4). MOSFET M_3 is used for the set and reset operations of R_n. Fig.5 shows simulated waveforms for the reset and successive set operations, in which gate bias V_W^{set} of M_3 is applied for a current compliance. The set resistance (R_n^{set}) of R_n can be modulated by V_W^{set}, as shown in Fig.6. The resistance values are also altered by gate width W_{nw} of M_3 (Fig.6). Fig.7 shows the transfer characteristics of the proposed gate. By adjusting R_n^{set}, logical threshold voltage V_T can be varied. The maximum modulation range of 114mV was obtained, when $W_{nw}/L = 2$, as shown in Fig.8. This V_T modulation can be applied to compensate variability of MOSFET characteristics. Fig.9 shows the results, where the threshold voltages shift of $\Delta V_{thn} = \pm 50$mV and $\Delta V_{thp} = \pm 50$mV are intentionally introduced for M_2 and M_1, respectively, to reproduce characteristics variation in the CMOS gate. The V_T shifts can be compensated by adjusting R_n^{set}, as shown in Fig.9.

Fig.10 shows a VT-CMOS inverter gate using complementary F-MOSFET architecture, where RSDs are introduced into both the source terminals of the n- and p-channel MOSFETs in the figure. This VT-CMOS gate can tackle to compensate much higher variability, compared with the VTCMOS gate shown in Fig. 4. The set resistance values (R_n^{set} and R_p^{set}) of R_n and R_p can be modulated by V_{W1}^{set} and V_{W2}^{set}, respectively, in the same manner as the VTCMOS inverter of Fig.4. From our calculations, a maximum V_T-modulation range of 232mV was achieved, when $W_{nw}/L = 2$ and $W_{pw}/L = 3.56$. Fig. 11 shows the results of variability compensation, where $\Delta V_{thn} = \pm 100$mV and $\Delta V_{thp} = \pm 100$mV are intentionally introduced. The wide range of V_T variations can be compensated by adjusting R_n^{set} and R_p^{set}, as shown in Fig.11.

Fig. 12 shows a VT-SRAM cell using VT-CMOS gates. Since V_T variations in the two cross-coupled inverters of the cell can be tuned by the constituent F-MOSFETs, the inverters mutually have the identical characteristics. Therefore, enough static noise margins for assured SRAM operation are realized

5. Conclusions

We proposed and analyzed VT-CMOS gates using F-MOSFETs with RSDs. They would be useful for assured CMOS operation ofsub-100nm CMOS circuits including characteristics variability.

References

[1] T. Kuroda *et al.*, *IEEE J. Solid-State Circuits* **31** (1996) 1770.

[2] K. Tsunoda *et al.*, *IEDM Tech. Dig.*, 2007, pp. 767-770.

[3] Device Group at UC Berkeley, "Berkeley Predictive Technology Model," BSIM3v3 parameter-set.

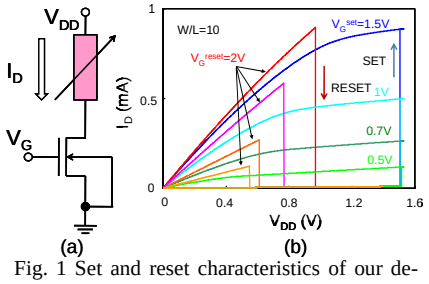

Fig. 1 Set and reset characteristics of our developed RSD model. (a) Examined circuit and (b) calculated characteristics.

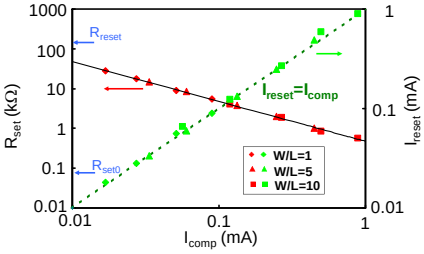

Fig. 2 Simulated R_{set} and I_{reset} as a function of I_{comp}.

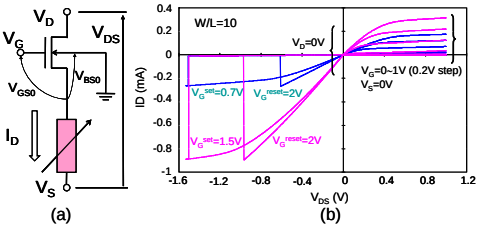

Fig. 3 (a) Circuit configuration of the proposed F-MOSFET, and (b) its current-voltage characteristics.

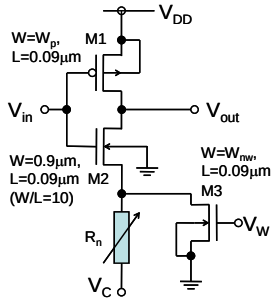

Fig. 4 Circuit configuration of a variability-tolerant CMOS (VT-CMOS) inverter gate.

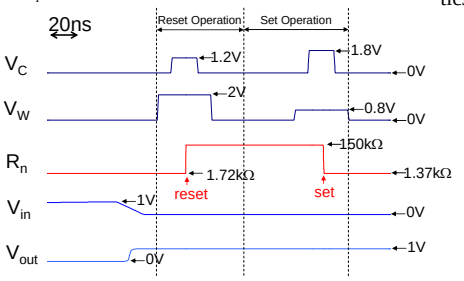

Fig. 5 Simulated waveforms of reset and set operations.

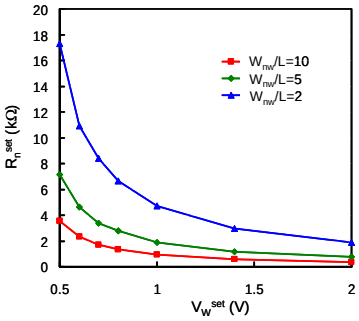

Fig. 6 V_W^{set}-dependence of set resistance (R_n^{set}).

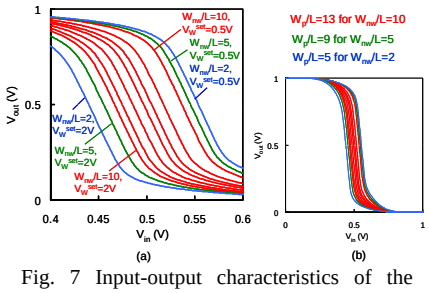

Fig. 7 Input-output characteristics of the proposed VT-CMOS inverter.

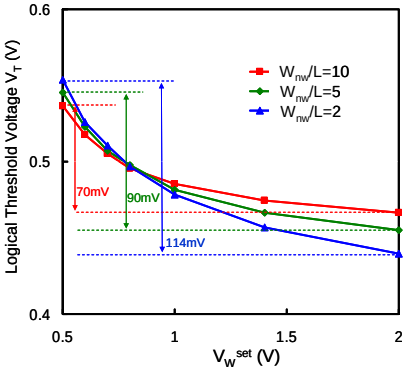

Fig. 8 Logical threshold voltage (V_T) of the proposed VT-CMOS inverter.

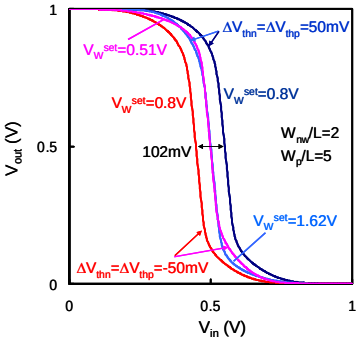

Fig. 9 V_T variability compensation characteristics

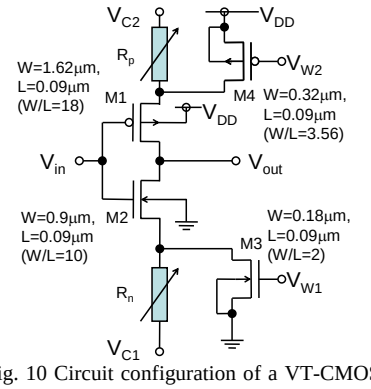

Fig. 10 Circuit configuration of a VT-CMOS inverter with two RSDs.

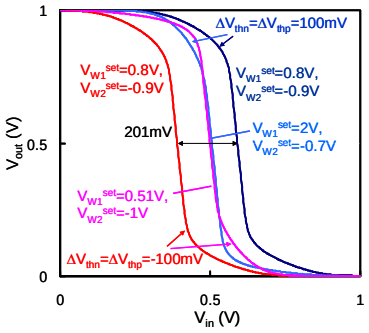

Fig. 11 V_T-variability compensation characteristics

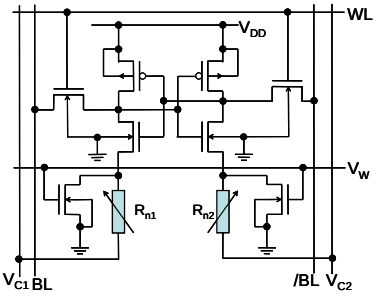

Fig. 12 Circuit configuration of a variability-tolerant SRAM.