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Characteristic Sensitivity of Multi-Gate and Multi-Fin MOSFETs to Random Dopant Fluctuation and Implication for Digital Circuits

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1. Introduction

As the gate length of bulk metal oxide semiconductor field effect transistor (MOSFET) shrinks below 32 nm, devices with vertical channel have drawn people's attention due to diverse fascinating characteristics [1-5]. Multi-fin FETs have thus been proposed to provide a large driving capability [3-5]. In this work, we explore DC and dynamic behavior of 16-nm-gate multi-fin transistors and digital circuits, with respect to different fin aspect ratio (AR = fin height (H_{fin}) / effective fin width (W_{fin})). Effect of AR on the random-dopants-fluctuation (RDF) induced characteristic fluctuations for devices and circuits including V_{th}, gate capacitance, delay time, and static noise margin (SNM) are further estimated.

2. Multi-Gate and Multi-Fin Devices and Circuits

Fig. 1(a) shows the examined triple-fin MOSFETs, without loss of generality. Devices are with different AR, where AR of FinFET, tri-gate MOSFET and quasi-planar MOSFET are two, one and 0.5, respectively, as shown in Fig. 1(b). The inset table of Fig. 1(b) lists the device setting. For comparison on a fair basis, cross-sectional area of the silicon fin for the explored devices is fixed at 128 μm^2. Additionally, the threshold voltages (V_{th}) of 32-nm-gate devices are first calibrated to 200 mV for the V_{th} roll-off characteristics. The similar cross-sectional area and V_{th} indicate the same control volume of device channel under the same operation condition. The device characteristics are simulated by solving a set of 3D density-gradient equations coupled with Poisson equations as well as electron-hole current continuity equations under our parallel computing system. Fig. 1(c) shows the SRAM and inverter circuits with the adopted multi-fin devices. Since no well-established SPICE model of such ultrasmall nano-devices is available, to capture the transfer and transient characteristics of the digital circuits including the RDF-induced characteristic fluctuations, a physically-sound coupled device-circuit simulation approach is advanced [6]. The physical models adopted in the device equations were calibrated with the fabricated and measured samples for the best accuracy [1, 7].

3. Results and Discussion

Fig. 2(a) plots the V_{th} roll-off for single- and triple-fin transistors with respect to different ARs. The gate length of devices varies from 32 nm to 16 nm. The preliminary results of this study show that multi-fin FinFETs structure with AR = 2 is less sensitive to the gate length scaling due to the larger effective device width ($W_{eff} = H_{fin} + 2xW_{fin}$). Notably, the effective fin width is increased as the number of fins is increased. The moderate V_{th} roll-off of FinFET implies superior channel controllability and resistance to intrinsic parameter variations. Fig. 3(a) plots the gate capacitance (C_g) of the 16-nm-gate single- and triple-fin devices; the triple-fin devices are about three times larger than that of single-fin devices. Compared with the triple-fin quasi-planar devices, C_g of triple-fin FinFETs is increased by a factor of 3.7. The large C_g of multi-fin transistor with a large AR enhances charge control; nevertheless, the increased C_g affects the operation speed of transistors. The intrinsic gate delay of transistor ($\tau = C_gV_{DD} / I_{on}$) is thus calculated, as shown in Fig. 3(b), to study the trade-off between I_{on} and C_g. The single-fin FinFET also presents a 2.5 and 1.1 times smaller τ than tri-gate and quasi-planar MOSFETs. The intrinsic gate delay is dominated by C_g; therefore, the use of multi-fin structure degrades the τ by 1.4 times, which may limit the applicability of multi-fin devices on high-frequency integrated circuits. Figs. 4(a) and 4(b) plot the high-to-low transition characteristics for both the single- and triple-fin devices inverters with respect to different AR, where transistors' intrinsic C_g is used as the load capacitance (C_{load}). The solid lines are the output signals of devices with different fin structure; the dotted line is the input signal. The high-to-low delay time (t_{HL}) is defined as the difference between the times of the 50% points of the input and output signals during the falling of the output signals. The high-to-low delay time (t_{HL}) of the studied single- and multi-fin transistors are summarized in inset of Figs. 4(a) and 4(b), respectively. As expected, both single- and multi-fin FinFET inverters present smallest t_{HL} with respect to different ARs, and show the beneficial of FinFET structure in both DC and dynamic characteristics. The multi-fin transistor provides a smaller transition delay than that of the single-fin transistor due to increase of driving current. Furthermore, different external C_{load} is added on the inverter circuit to examine the associated delay time, as shown in Figs. 5(a) and 5(b), respectively. The delay time increases significantly as C_{load} increases. The C_{load} dominates the overall C_{load}, where the difference of device intrinsic load capacitance (i.e., intrinsic C_g) caused by the fin structure becomes negligible. For the triple-fin FinFET inverter with a 10 fF C_{load}, its delay time is about two times smaller than that of the single-fin FinFETs. Besides, device variability is also crucial for digital circuits; by considering an intrinsic C_g as the load capacitance, Fig. 6 examines the RDF-induced σV_{th}, and σC_g of the multi-fin devices. The σV_{th} of p-FET is smaller than n-FET, the σV_{th} of n-type FinFET and p-type FinFETs are 1.5 and 1.9 times smaller than that of quasi-planar structures, which indicates that under the same channel volume, the FinFET possesses more uniform surface potential. The σC_g of multi-fin FinFETs is increased slightly due to the increased gate area. The inset of Fig. 6(b) shows the normalized on-state current fluctuation ($\sigma I_{on} / I_{on}$). Though σC_g of multi-fin FinFETs is increased slightly, the large and stable on-state current reduce $\sigma\tau$ of FinFET, as shown in Fig. 7(a). Figure 7(b) presents σt_{HL} and σt_{LH} of multi-fin device inverters. The σt_{HL} and σt_{LH} are dominated by n-FET and p-FET, respectively. Thus σt_{HL} exceeds σt_{LH} due to a larger σV_{th} of n-FETs. The SNM of multi-fin devices SRAM cells is further examined, as shown in Fig. 8(a). The FinFET exhibits the largest SNM among the explored device structures. Figure 8(b) presents the RDF-induced SNM fluctuation (σ_{SNM}) of the multi-fin devices SRAM cells. Because of the smallest V_{th} fluctuation, the multi-fin FinFETs shows the largest SNM and smallest σ_{SNM}. The normalized σ_{SNM} are summarized in inset of Fig. 8(b).

4. Conclusions

This study examined DC and transient behavior of single- and multi-fin vertical channel devices and circuits with different AR. In single-fin transistor, FinFET offer a 1.2 and 1.3 times smoother roll-off characteristics than tri-gate and quasi-planar MOSFETs. By using multi-fin structure, the roll-off characteristics is further reduced by 1.8 times. In digital circuits, owing to the large driving capability, the single-fin FinFET inverter shows a 2.2 and 2.5 times smaller t_{HL} than tri-gate and quasi-planar MOSFETs. The t_{HL} is further reduced by 1.4 times in multi-fin FinFET structure. For the RDF in multi-fin transistors, comparing to the quasi-planar MOSFETs, the use of FinFET structure reduce the σV_{th}, normalized σI_{on}, σC_g, $\sigma\tau$, σt_{HL} , σt_{LH}, and normalized σ_{SNM} by 1.5, 1.2, 0.88, 2.4, 1.7, 1.8, and 3.2 times. Though the σC_g is increased due to the larger depletion region, the stable current flow enhances the reliability of timing and SNM characteristics. The multi-fin FinFET presents a better channel controllability, driving current, timing characteristic, SNM and their fluctuation resistivity than other structures with the smaller ARs.

Acknowledgement

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References

[1] Y. Li *et al.*, IEEE Trans. Electron Devices **54** (2007) 3426.
[2] Y. Li *et al.*, J. Appl. Phys. **102** (2007) 084509.
[3] B. Swahn *et al.*, IEEE Trans. VLSI **16** (2008) 816.
[4] H. Shang *et al.*, in Digest of Symp. VLSI Tech. (2006) 54.
[5] S. M. Kim *et al.*, in IEDM Tech. Dig., (2004) 639.
[6] Y. Li *et al.,* IEEE Trans. Microw. Theory Tech., **56** (2008) 2726.
[7] Y. Li *et al.,* IEEE Trans. Electron Devices **55** (2008) 1505.

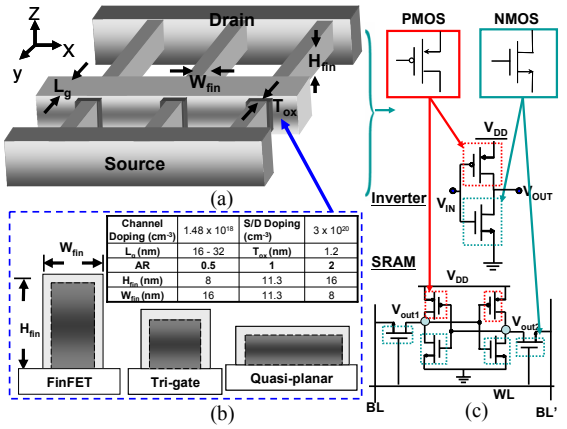

Fig. 1. (a) A schematic and (b) cross-sectional view plots of the multi-fin MOSFET. There have three fin shapes which are FinFET (AR = 2), tri-gate (AR = 1) and quasi-planar (AR = 0.5), respectively. The parameter settings are presented in inset tables. (c) Inverter and SRAM are used as the test circuits. BL and BL' are bit lines; WL is the word line.

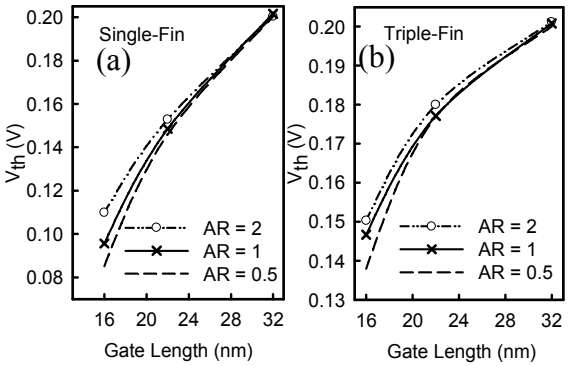

Fig. 2. Plot of V_{th} roll-off characteristics for (a) single-fin and (b) triple-fin MOSFETs with respect to different fin aspect ratio.

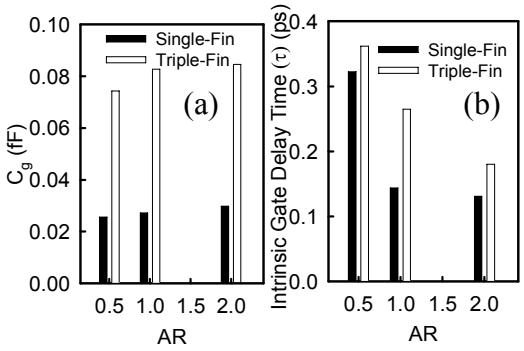

Fig. 3. The (a) device gate capacitance and (b) the intrinsic gate delay for the studied single- and multi-fin transistor with different AR.

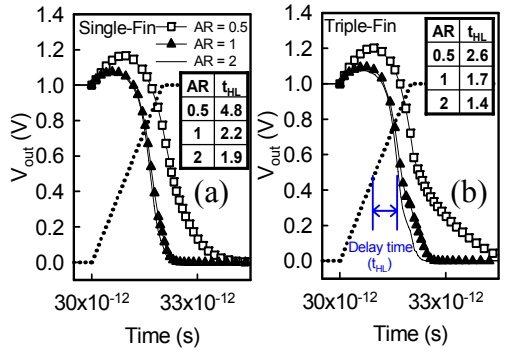

Fig. 4. The transient characteristics for (a) single- and (b) multi-fin inverters, where the extracted rise time, fall time, and hold time of the input signal are 2 ps, 2 ps, and 30 ps, respectively.

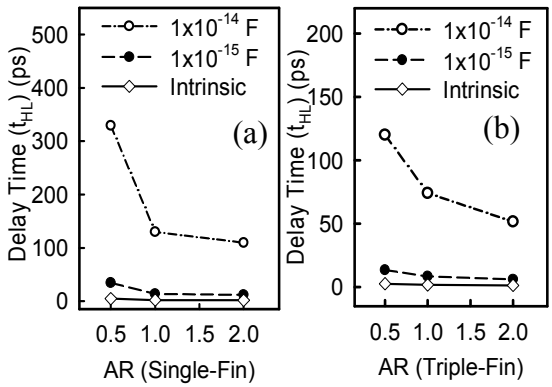

Fig. 5. The delay time for (a) single- and (b) multi-fin inverters with the intrinsic and 1x 10^{-14} F and 1x 10^{-15} F external load capacitances.

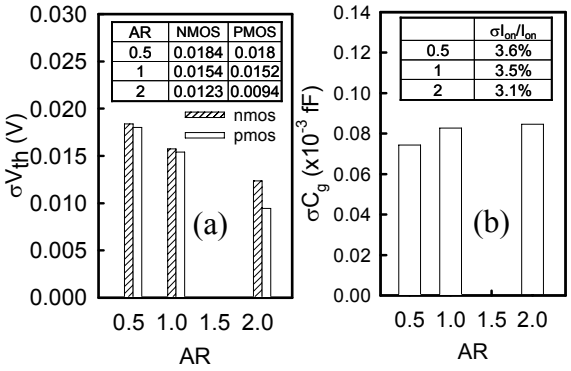

Fig. 6. The (a) σV_{th} and (b) σC_g of multi-fin transistors with various. The inset of (a) and (b) shows the summarized σV_{th} and normalized on-state current fluctuation (σI_{on} / I_{on}).

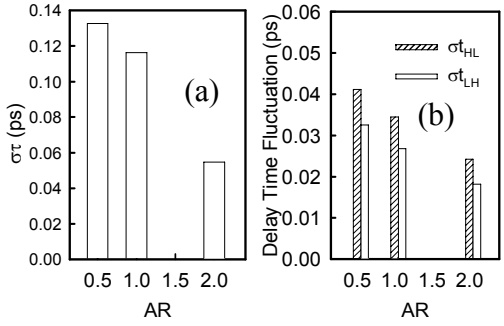

Fig. 7. (a) The $\sigma\tau$ of multi-fin transistors. (b) The σt_{HL} and σt_{LH} of the tested inverter with AR = 2, 1 and 0.5, respectively.

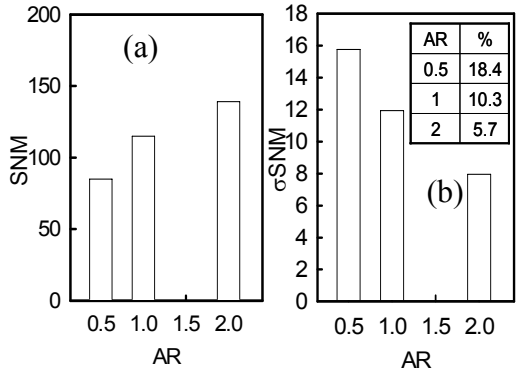

Fig. 8. (a) The SNM and (b) SNM fluctuation of the examined SRAM with AR = 2, 1 and 0.5, respectively.