

Excellent stability of GaN-on-Si HEMTs with 5 μm gate-drain spacing tested in off-state at a record drain voltage of 200 V and 200 $^{\circ}\text{C}$

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1. Introduction

Environmentally friendly technologies intrinsically require high efficiency devices to avoid energy losses. In particular, applications such as radio frequency (RF) power amplifiers for base stations, power switches in solar converters or in hybrid vehicles are suffering from the low efficiency of Si-based devices.

Today, gallium nitride (GaN) based devices are receiving large attention since they combine high voltages and frequency capabilities, high current density and low on-resistance (R_{ON}) [1] - [3]. These are the key-factors to enable “green” high-voltage power devices for RF or switching applications. In particular, large attention is focused on gallium nitride High Electron Mobility Transistors grown on Si substrate (GaN-on-Si HEMTs). They combine high performance [3], [4] with the possibility of processing large-diameter wafers, up to 200 mm [5]. This results in a high performance low cost technology.

In contrast to the large amount of publications reporting impressive performance of GaN-based devices, the number of reliability studies is relatively small [6]-[8]. It is reported that stability problems might rise when the device is biased in off-state at high drain voltage during the operation. Such conditions induce a very high electric field peak under the gate edge on the drain side. Consequently, despite the intrinsic high voltage capabilities, reliability issues might limit the operating bias.

In order to investigate the high electric field degradation phenomena, in this work we focus on small gate-drain spacing. Clearly, the larger the gate-drain distance, the lower the electric field peak for a given drain voltage.

To our best knowledge we report the highest voltage/temperature stability test of GaN-on-Si HEMTs with a gate-drain spacing (L_{GD}) of 5 μm . Several transistors were stressed for more than 100 hours in pinch-off conditions ($V_{\text{GS}} = -7 \text{ V}$) at a drain voltage (V_{DS}) up to 200 V and at the same time at high ambient temperature (T_{CHUCK}) of 200 $^{\circ}\text{C}$. Remarkably, the devices under test showed negligible degradation.

2. Experiment Description

Device Description

In order to obtain high breakdown voltage devices, an AlGaIn/GaN/AlGaIn double heterostructure configuration

was used [9], [10]. The key features of this configuration are the better electron confinement combined with the larger breakdown voltage of the AlGaIn layer below the channel as compared to the commonly used GaN/AlGaIn single heterostructure.

The epitaxial layer was grown by Metal-Organic chemical vapor deposition (MOCVD) on Si (111) substrate. The stack consists of a 2 μm thick AlGaIn buffer layer, 150 nm GaN channel layer and a 22 nm $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$ barrier layer. Afterwards, 50 nm of Si_3N_4 was deposited in-situ, in order to passivate surface states and to prevent cracks in the barrier layer due to the lattice mismatch with the channel layer [11], [12].

Device isolation was obtained by mesa etching using Cl_2 based chemistry. In order to achieve a low access resistance, the ohmic contacts were fabricated after selectively removing the in-situ Si_3N_4 layer by SF_6 -based etching. The ohmic contact metallization was formed by depositing Ti/Al/Mo/Au followed by rapid thermal annealing at 850 $^{\circ}\text{C}$. The same etching recipe was also used to define the gate foot in the in-situ dielectric layer. The gate metallization was Ni/Au (20 nm/200 nm) which results in a T-shape gate. Finally an extra ex-situ passivation of 200 nm of Si_3N_4 was deposited.

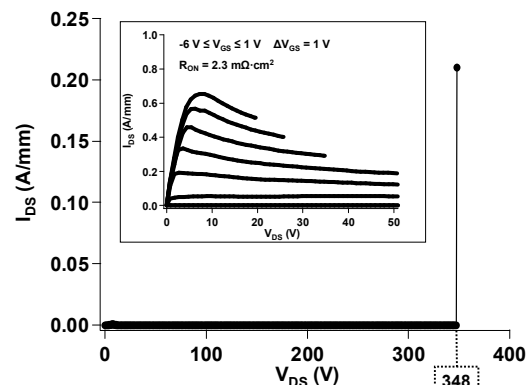


Fig. 1. Off-state ($V_{\text{GS}} = -7 \text{ V}$) breakdown measurement. The breakdown voltage is 348 V. The inset shows a typical output $I_{\text{DS}}-V_{\text{DS}}$ characteristic.

Large attention was dedicated to the gate process step, in particular in the etching recipe to avoid plasma induced defects and ion implantation. Indeed, we observed that an immature gate technology might lead to process-induced

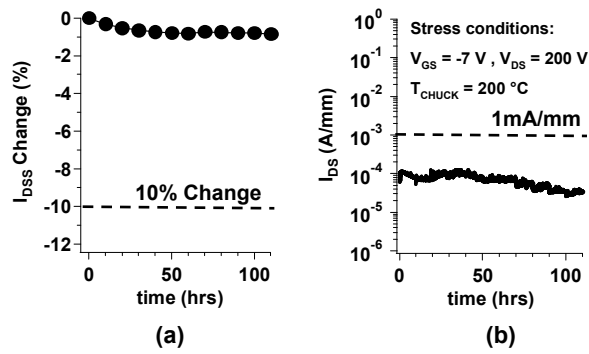


Fig. 2. (a) I_{DSS} variations at 200 °C relative to the fresh value measured every 10 hours by interrupting the stress for few seconds; (b) drain leakage current measured during the stress at the conditions indicated in figure; the failure criterion is indicated in both figures with a dash line.

failures, then low yield and poor reliability [13].

The device geometries used for this study were: gate length $L_G = 1.5 \mu\text{m}$, field plate length $L_{FP} = 1 \mu\text{m}$, gate-source spacing $L_{GS} = 1.5 \mu\text{m}$ and gate-drain spacing $L_{GD} = 5 \mu\text{m}$. The device width was $W = 0.2 \text{ mm}$

The drain-source saturation current (I_{DSS}) measured at $V_{DS} = 5 \text{ V}$ and $V_{GS} = 0 \text{ V}$ was 580 mA/mm (inset Fig. 1). The off-state device breakdown was more than 300 V (Fig. 1) with the specific R_{ON} as low as $2.3 \Omega\cdot\text{cm}^2$.

Measuring Procedure

Several devices were DC-stressed in off-state ($V_{GS} = -7 \text{ V}$) at high drain voltage up to $V_{DS} = 200 \text{ V}$ for more than 100 hours. The ambient temperature was set to 200 °C in order to accelerate a possible degradation.

A complete characterization was done before and after the stress both at room and at stress temperature. The drain leakage current was measured every 2 s during the stress test.

Moreover, the bias stress was switched off every 10 hours in order to extract the I_{DSS} as defined above. Indeed, the failure criteria were defined as a 10 % drop of I_{DSS} compared to the initial value or an increase of the drain leakage current above 1 mA/mm. It is reported that one of the first degradation signs is a change of at least one of these two parameters [6]-[8].

3. Results

Fig. 2a shows the I_{DSS} variation at 200 °C whereas in Fig. 2b the I_{DS} leakage current during the stress is plotted. Both parameters remained relatively stable and far from the commonly accepted failure levels defined above.

The excellent reliability of our gate process technology is confirmed by the fact that no abrupt increase of the leakage current is observed (Fig. 2b) during the entire 200 V stress period.

Moreover, the effectiveness of the in-situ Si_3N_4 passivation is proven by the negligible drop of less than 1% of the I_{DSS} (Fig. 2a). We attribute this drop to a small trapping effect (e.g. coming from the final extra passivation layer) since it is observed only in measurements done immedi-

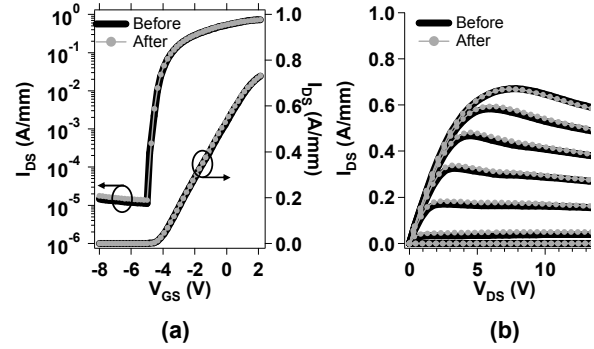


Fig. 3. DC characteristic before (black line) and after stress (grey line and circle markers) measured at room temperature; (a) I_{DS} - V_{GS} characteristic in linear and semi-log scale measured at $V_{DS} = 10 \text{ V}$; (b) I_{DS} - V_{DS} characteristic measured from $V_{GS} = -6 \text{ V}$ to $V_{GS} = 1 \text{ V}$ with step of $\Delta V_{GS} = 1 \text{ V}$.

ately after the stress at 200 °C. Indeed, measurements performed after cooling down to room temperature (Fig. 3a and Fig. 3b) show no change in the I_{DSS} and in the other device parameters: the threshold voltage, sub-threshold slope, leakage current and R_{ON} remain constant.

4. Conclusion

For the first time, GaN-on-Si HEMTs with small gate-drain distance ($5 \mu\text{m}$) were stressed for more than 100 hours in off state at 200 V and 200 °C. We showed that the combination of high quality AlGaIn/GaN/AlGaIn double heterostructure, in-situ Si_3N_4 deposition and an accurately optimized gate process technology resulted in excellent device stability.

Remarkably, negligible change of the transistor characteristic was observed. Stress measurement for longer time is on-going and will be reported later.

This work shows that GaN-on-Si HEMTs could be a highly reliable cost-effective technology for the next generation of “green” (high efficiency) high-voltage power devices for switching and RF applications.

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