

## Defect-free Isolation on High-Thermal-Conductivity SOI Substrates for Complementary BiCMOS Technology

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**Abstract** – In this paper, we present our first experimental results of 200mm bonded “High-Thermal-Conductivity” (HTC) SOI substrate fabrication using the SiO<sub>2</sub>-Si<sub>3</sub>N<sub>4</sub>-SiO<sub>2</sub> dielectric stack (ONO). Defect-free isolation was successfully obtained, applying standard SOI-CBiCMOS processing on these bonded ONO-HTC-SOI substrates.

### 1. Introduction

Literature has elaborated extensively on the fundamental restrictions/ limitations of standard SOI substrates for high power applications [1-5]. Indeed, in standard SOI, a SiO<sub>2</sub> layer separates the top mono-crystalline Si layer (that hosts the active device where the electrical power is dissipated into heat) from the bottom Si body that provides mechanical support during wafer handling and a medium to conduct heat towards the heat sink. The SiO<sub>2</sub> however, is a poor thermal conductor and impedes heat evacuation from the device towards the drain. In consequence, junction/device temperature rises in high power operation (device self-heating and thermal runaway). The Safe Operation Area (SOA) is reduced in comparison to bulk Si substrates, worsening with thicker buried oxide.

In a previous publication [1], we discussed a possible solution to overcome this electro-thermal issue from simulation point of view. The buried SiO<sub>2</sub> of the bonded SOI substrate is replaced by a sandwich structure of which the sub-layers are selectable and optimized individually in thickness in order to meet the specifications to enable the bonding process on one hand and result in better thermal conduction on the other hand, without excessively deteriorating parasitic capacitive coupling and jeopardizing high speed performance of the active device.

In this work, we present our first experimental results, demonstrating this concept in the context of (Complementary) BiCMOS Technology for integrated RF circuits. The paper is composed of following parts:

- Selection and preparation of sandwich stacks
- Bonding process
- Introduction of bonded HTC-SOI substrates in IMEC’s 8 inch (200mm) pilot line and processing of first process modules (buried layers, collector epi, shallow and deep trench isolation) for the fabrication of high speed SiGe npn and pnp heterojunction bipolar transistors (HBTs) on HTC-SOI.

### 2. Selection of the multilayer composition and Handle wafer preparation (prior to bonding)

We have experimentally investigated several materials (stacked with a thin SiO<sub>2</sub> layer), among others undoped polycrystalline Si, amorphous Si, Si<sub>3</sub>N<sub>4</sub>, AlO<sub>3</sub>, AlN and SIPOS. Some materials show too much surface roughness for subsequent bonding. In this case, a Chemical Mechanical Polishing (CMP) step of the layer or capping (+ CMP) is required. Secondly, some deposited materials cause too large wafer bow for the subsequent bonding, especially for single side depositions. This wafer bow worsens with layer thickness but can be compensated by adequate backside depositions. Finally, the stack must be delivered to bonding with low particle levels and low surface contamination. So, a proper cleaning step may be necessary.

Here, we present our recent work combining SiO<sub>2</sub> (O) and Si<sub>3</sub>N<sub>4</sub> (N) to make an ONO-HTC-SOI substrate. We used 100nm, 200nm or 400nm of Si<sub>3</sub>N<sub>4</sub> sandwiched by 20nm thermal oxide, and 10nm TEOS on top. The choice of ONO is trivial. It offers a first improvement in thermal conductivity (wrt. SiO<sub>2</sub>-only) [1, 6] and it is relatively easy to implement for following reasons.

Surface micro roughness of the stack, as measured by AFM, is very low and hardly depending on layer thickness since SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> are amorphous (Fig. 1). No CMP is required to meet the spec. of 0.5nm rms.

Secondly, wafer bow is acceptable since oxidations/ depositions are performed in furnaces and therefore simultaneously on front and back side. For wafer bonding, it is preferable that the wafer bow of the handle and donor wafers be less than 30μm. This spec. is also fulfilled, as shown in Fig. 1.

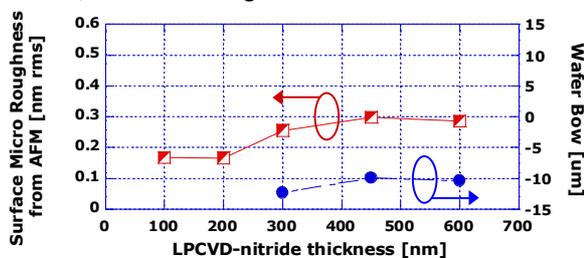


Figure 1. Surface micro roughness and wafer bow of ONO stacks as function of Si<sub>3</sub>N<sub>4</sub> layer thickness (Si<sub>3</sub>N<sub>4</sub> sandwiched by 20nm thermal SiO<sub>2</sub> and 10nm TEOS)

However, mismatch of thermal expansion coefficients of  $\text{Si}_3\text{N}_4$  and Si and high Young's modulus of  $\text{Si}_3\text{N}_4$  may result in Si crystal defect generation during device processing and unacceptably high junction leakage current. Absence of crystal defects is therefore crucial.

### 3. Wafer bonding

Wafer bonding, layer-transfer, and epitaxial growth were applied to fabricate BiCMOS compatible SOI wafers with the ONO dielectric sandwich. Although feasibility was demonstrated to use the ONO coated wafers as either a handle or donor, the SOI wafers of this study were fabricated with the ONO coated wafer used as the handle wafer. Key aspects of the SOI process development for the ONO sandwich included the pre-bonding surface preparation of the ONO handle wafer and donor wafer, optimization of the plasma activated bonding conditions, and the control of bubble formation at the bond interface during thermal processing after bonding and layer-transfer.

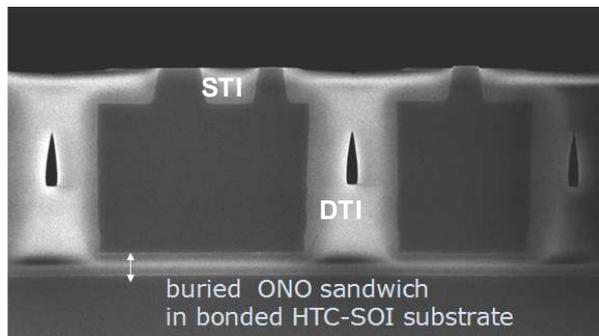


Figure 2. XSEM without sample preparation (after As BLN I/I, epi growth, STI and DTI); ONO stack with 200nm  $\text{Si}_3\text{N}_4$

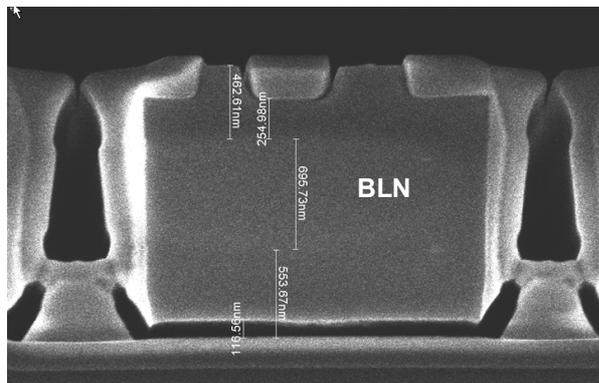


Figure 3. XSEM after SECCO-etch sample preparation (after As BLN I/I, epi growth, STI and DTI processing)

### 4. Buried Layers and Defect-free Isolation

The 8 inch ONO-SOI substrates received initially buried collector implantation (BF2 for pnp BLP and As for npn BLN), followed by oxidation and thermal annealing to remove damage and activate the doping, oxide removal in HF and epitaxial growth of  $\sim 1\mu\text{m}$  to bury the implanted regions. We used standard SOI-CBiCMOS process conditions that result in BLN Rs of  $\sim 20\text{ Ohm/sq}$

and BLP Rs of  $\sim 50\text{ Ohm/sq}$ . At this stage, XSEM inspections were done after applying SECCO-etch for crystal defect decoration. No defects were observed so the remaining wafers continued through Shallow Trench Isolation (STI) and Deep Trench Isolation (DTI) processing. The std. SOI-CBiCMOS deep trench Si etch process is sufficiently selective to stop on the top oxide of the buried stack. These deep trenches ( $0.6\mu\text{m}$  wide) reach down to the buried ONO and are oxide filled (oxide liner, HDP oxide, annealed TEOS). The isolation module ends with CMP for planarization and wet removal of padoxide/ nitride that protect the active regions during CMP. Again, no defects were observed in cross section (after applying SECCO-etch that was proven to be effective on a witness sample), cf. Fig. 2-3.

### 5. Conclusions

HTC-SOI substrates have been realized using a conventional dielectric ONO stack to replace  $\text{SiO}_2$ . These substrates were successfully introduced in the IMEC pilot line, first process modules were completed and defect-free isolation was obtained. Standard process modules have been used so far which proves the good portability of our std. SOI-CBiCMOS process. It is not expected to meet major process issues or showstoppers during the remainder of the process flow.

Further work consists of completing the fabrication of SiGe npn and pnp HBTs on HTC-SOI in order to evaluate the DC and RF operation at high power, to extract the thermal resistance from the  $I_c$ - $V_{ce}$  output curves and benchmark the thermal performance to the corresponding HBT device on a standard SOI substrate. The initial  $R_{th}$  simulations [1] can then be validated, stability of thermal material properties of the ONO stack during the whole fabrication process studied and the impact of interfaces on  $R_{th}$  accurately modeled. Finally, many other sandwich combinations (also including more exotic materials that are adequately capped and/or polished and cleaned) with higher thermal conductivity than  $\text{Si}_3\text{N}_4$  need to be further explored.

### Acknowledgments

The MEMC and IMEC Production and Material characterization teams are gratefully acknowledged for realizing all processing and sample analysis.

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