Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp826-827

Effect of drain bias stress on the stability of nanocrystalline silicon thin film transistor with various channel length

Sun-Jae Kim, Sang-Geun Park, Seon-Beom Ji and Min-Koo Han

School of Electrical Engineering and Computer Science, Seoul National University,
599 Gwanangno, Gwanak-gu, Seoul, 151-742, KOREA
Phone: +82-2-880-7992 Fax : +82-2-871-7992 E-mail: sjglory@emlab.snu.ac.kr

1. Introduction

Nanocrystalline silicon (nc-Si) thin film transistor (TFT) has attracted considerable attention for various applications such as display and image sensor [1]. It can be fabricated with rather simple process as compared with polycrystalline silicon (poly-Si) TFT since it doesn't require additional recrystallization process. It also exhibits better uniformity while recrystallization process causes troublesome non-uniformity problem in poly-Si TFT [2,3]. nc-Si TFT also has advantage compared to hydrogenated amorphous silicon (a-Si:H) TFT due to better electrical stability [4].

Several works have reported the stability of nc-Si TFT.[5-7] However, most of reports focused on the stability under gate bias stress only. Since the TFT used as a current source in AMOLED pixel arrays have a bias at the drain terminal in addition to the gate, we have to consider the drain bias stress to the TFT.

The purpose of our work is to report the effect of drain bias on the degradation of nc-Si TFTs with various channel length.

2. Experimental

We have fabricated nc-Si TFTs of an inverted staggered structure. Molybdenum was sputtered with thickness of 2000 Å on the glass substrate and patterned as gate metal. SiN_X of 4000 Å was deposited and nc-Si film of 2000 Å was deposited.

ICP-CVD was employed for the deposition of nc-Si film. ICP-CVD provide certain advantages such as high deposition rate and improved crystallinity of nc-Si film, can be used for fabrication of high quality nc-Si TFTs. ICP-CVD employs remote plasma, which reduces troublesome ion bombardment problem issues.

The process temperature of the deposition was set to 350 ^{o}C. Helium gas was used for the dilution of the reactant gas. The flow rate of Helium : Silane (SiH_4) was 40:3 [sccm]. The base pressure in the reactor was less than 1 mT and the process pressure during the deposition was set to 50 mT and the ICP power was 700W.

The 500Å-thick n+ layer was deposited and the active patterning was carried out. 2000Å- thick molybdenum as the source/drain metal was sputtered and patterned. The n+ layer on the channel region was etched. The thicknesses of channel region were remained about 700 Å after etch-back process. Fig. 1 shows the cross-sectional TEM images of the fabricated nc-Si TFT. It shows the interface between nc-Si and SiN_X. Clear silicon lattice patterns are observed right on the SiN_X layer, which implies that the incubation layer of amorphous phase is not formed during the nc-Si deposition. I-V characteristics of the TFTs with width=90 μm and various lengths were measured.

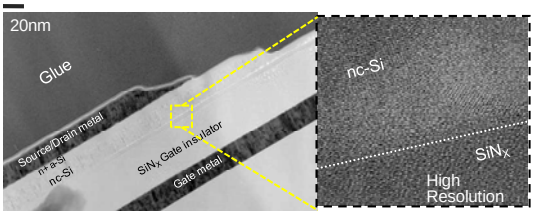

Fig. 1 The cross-sectional TEM images of the fabricated nc-Si TFT and high resolution cross-sectional TEM image showing the interface between nc-Si and SiN_X.

3. Results and Discussion

Fig.2 shows the transfer characteristic of the nc-Si TFT. The field effect mobility at V_{DS} of 0.1V, the threshold voltage (V_{TH}), subthreshold slope and on/off ratio were 0.77 $cm^2/V{\cdot}sec$, 3.69 V, 1.66 V/dec and $\geq 1\times10^6$, respectively.

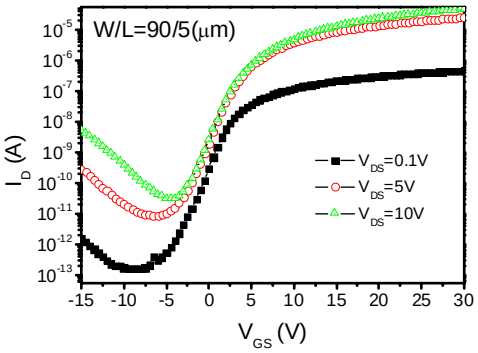

Fig. 2 The transfer characteristic and the output characteristic of fabricated nc-Si TFT

Fig. 3 shows the V_{TH} shift of the nc-Si TFT (W/L=90/5) in the presence of drain bias stress. As the bias at the TFT drain terminal increases from 0V to 10V while gate bias is fixed to 15V, the V_{TH} shift of the nc-Si TFT decreases significantly. Also, in the presence of drain bias (V_G = 15 V, V_D = 10 V), V_{TH} shift decreased as the channel length reduced as shown in Fig. 4. The nc-Si TFT of 5 μm have smaller V_{TH} shift of 0.13 V than the 10 μm channel nc-Si TFT with V_{TH} shift of 0.67 V. In the TFTs with over 10 μm channel length, the V_{TH} shift was almost the same as that of 90 μm channel length TFT.

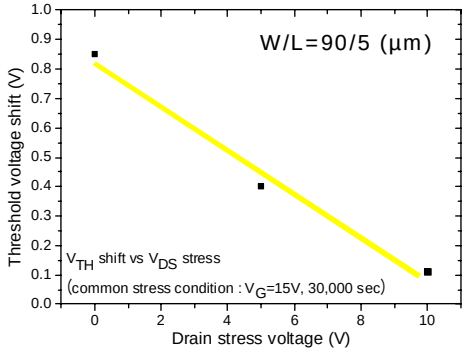

Fig. 3 V_{TH} shift of nc-Si TFT (W/L=90/5) with various drain bias stress (30,000 sec)

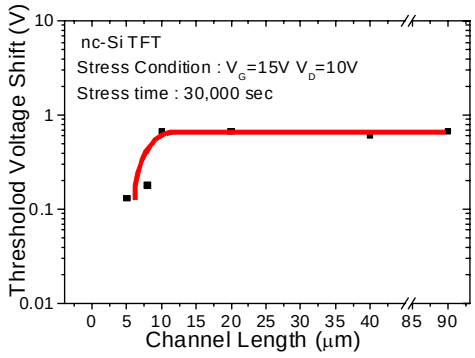

Fig. 4 V_{TH} shift with various channel length (stress condition: V_G=15V and V_D=10V)

Less V_{TH} shift in of the nc-Si TFTs can be explained by the concentration of the channel charge varying with the drain bias. As the drain bias increases, the carrier concentration in the channel decreases. Since the portion of the depleted charges over total charges increases with reducing channel length, the short channel TFTs have the smaller carrier concentration than the long channel TFTs.

Defect state creation can be characterized by a power law dependence of ΔV_{TH} over time, and ΔV_{TH} can be represented as follows [8]: $\Delta V_{TH}(t) = A(V_{ST} - V_{Ti})t^{\beta}$

(where A and β are temperature-dependent parameters, V_{ST} is the gate bias stress voltage, V_{Ti} is the V_{TH} of the TFT before bias stress is applied, and t is the bias stress time duration.)

When a bias is applied to the drain terminal, the carrier concentration in the channel decreases and consequently, less defect states are created so that the ΔV_{TH} decreases if the drain bias exists. Therefore, Eq. (1) can be modified as follows: $\Delta V_{TH}(t) = (\frac{Q_G}{Q_{G0}})A(V_{ST} - V_{Ti})t^{\beta}$ (Q_{G0} is the maximum channel charge, Q_G is the gate and drain bias-dependent channel charge, and Q_G/Q_{G0} is the normalized channel charge.)

Consequently, the V_{TH} degradation in short channel TFTs would be smaller than that of long channel TFTs under the same drain bias condition.

4. Conclusion

We have successfully fabricated nc-Si TFTs of bottom gate structure and evaluated their characteristics and electrical stability. Our experimental results showed that a short channel nc-Si TFT exhibited less degradation than a long channel TFT when the drain bias is applied. The less carrier concentration in a short channel TFT under drain bias creates less defect states, so that a short channel TFT exhibits less V_{TH} degradation than a long channel TFT.It can be expected that the nc-Si TFT with short channel length is reliable device for stable AMOLED display.

References

[1] J. H. Lan and J. Kanichi, *Tech. Digest of Int. Display Res. Conf. 1997*, pp. L58-L61, (1997).

[2] J. S. Im and H. J. Kim, *Appt. Phys. Lett*. Vol. 63 (14), pp. 1969-1971, (1993).

[3] M. Itoh, Y. Yamamoto, T. Morita, H. Yoneda, Y. Yamane, S. Tsuchimoto, F. Funada and K. Awane, *Tech. Digest of SID 1996*, pp17~20, (1996).

[4] K. Ichikawa, S. Suzuki, H. Maino, T. Aoki, T. Higuchi and Y. Oana, *Tech. Digest of SID 1999*, pp. 226-229, (1989).

[5] R. M. Esmaeili-Rad, A. Sazonov and A. Nathan, *IEDM '06*, pp1-4, Washington D.C.,USA, (2006).

[6] M. Oudwan, Y. Djeridane, A. Abramov, B. Aventurier, P.R.i. Cabarrocas and F. Templier, *Thin Solid Films* , 515, pp 7662-7666, (2007).

[7] A. Orpella, C. Voz, J. Puigdollers, D. Dosev, M. Fonrodona, D. Soler, J. Bertomeu, J. M Asensi, J. Andreu and R. Alcubilla, *Thin Solid Films*, Vol.395, pp335-338 (2001).

[8] C.-S. Chiang, J. Kanicki, K. Takechi, Jpn. J. Appl. Phys. 37 (1998)