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Metal-free Elementary Semiconductor Nanowires: Synthesis and Device Applications

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1. Introduction

Semiconductor nanowires are promising building blocks for various nanoscale devices since these materials can exhibit diverse device behavior and simultaneously function as the wires that access and interconnect devices [1]. In particular, nanowires of elementary semiconductors, such as Si and Ge, are a natural choice for the building blocks of future functional nanoscale devices because of their compatibility with existing silicon technology. So far, metal-catalyzed chemical vapor deposition (CVD) methods [2] have proven to be the most successful in producing various semiconductor nanowires and their related heterostructures, as the structures and electrical properties can be tailored in a wide range. However, the problem of metal contamination may apply to these nanowire devices, since metal impurities are unavoidable as long as metal-catalyzed growth approaches continue to be used. Contamination of nanowire/oxide interface by heavy metals, such as gold, would eventually be considered fatal to the long-term reliability of gate oxide because of the large diffusion constants of these metals. Also, metal-induced deep-level defects are efficient recombination and generation centers that have detrimental effects on the behavior of most electronic and optoelectronic devices.

Here, we report metal-free synthesis of high-density single-crystal elementary semiconductor nanowires with controls of diameters, morphology, growth direction and electrical conductivities [3].

2. Experiments and results

In our typical growth process of Si nanowires, a piece of H-terminated Si wafer was etched with ultrapure water to generate a reactive silicon-rich oxide (SiO_x) layer on the substrate surface. Si nanowire growth was initiated on the surface at 520 °C and 15 Torr using SiH_4 (10% diluted in H_2) for 2 min and then the anisotropic growth of the single-crystal nanowires was carried out at a reduced temperature of 490 °C for 10-30 min. Ge nanowires were also grown with a similar two-step growth method by the flow of a mixture of GeH_4 and H_2 gases. We note that the growth conditions are almost identical to that of the optimized condition for Au-catalyzed VLS growth of Si and Ge nanowires. Field emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM) images of typical as-grown Si and Ge nanowires on a planar silicon substrate show that highly dense nanowires were obtained with an aspect ratio (length/diameter) of more than 10^3 (Fig. 1). High-resolution TEM images and electron diffraction (ED) patterns of the Si and Ge nanowires show that most of the wires are single crystals (Figs. 1b and 1d). No metal catalyst was observed at the nanowire ends, confirming that the nanowire growth was not based on metal catalyst.

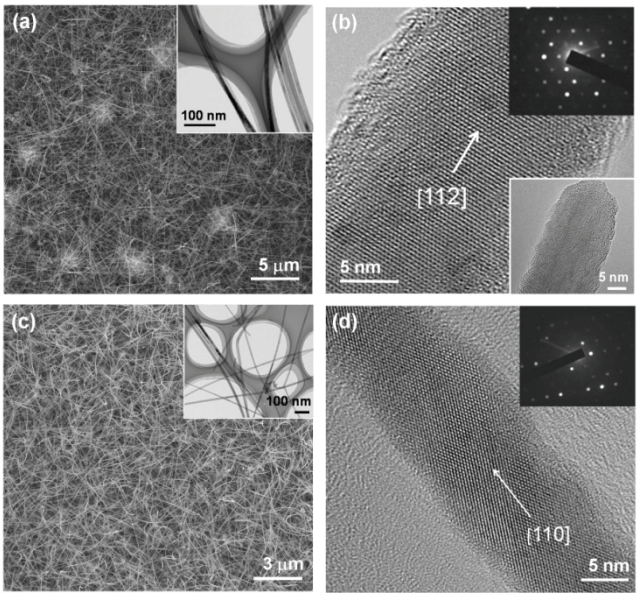
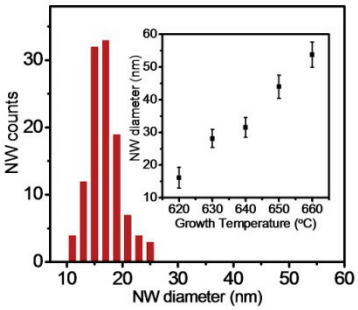


Fig. 1. (a) A typical SEM image showing high-density, uniform Si nanowires. (inset) A TEM image of the straight and uniform silicon nanowires. (b) Lattice-resolved TEM images taken at the middle and end (lower inset) of a single-crystal Si nanowire. (upper inset) The corresponding diffraction pattern (ED) recorded along the [111] zone axis. (c) SEM and low-magnification TEM images showing Ge nanowires. (d) A TEM image of a single-crystal Ge nanowire. (inset) The corresponding ED pattern

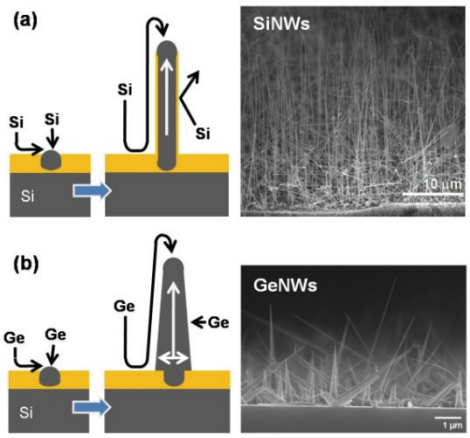
Optimum temperature range for growth of uniform single-crystal nanowires was quite narrow and the nanowires grown at higher temperature tended to be tapered and sheathed by nonspecific deposition of precursors. However, with additional flow of HCl, we were able to grow single-crystal wires without amorphous shell at much higher temperature in a relatively wide temperature range. Uniform metal-free Si nanowires were grown with additional HCl flow and the average diameter of the wires

increases in proportion to an increase in growth temperature with quite narrow diameter distributions (Fig. 2), which demonstrate that the diameter of these wires can be controlled without using pre-defined monodisperse metal nanoparticle catalysts.



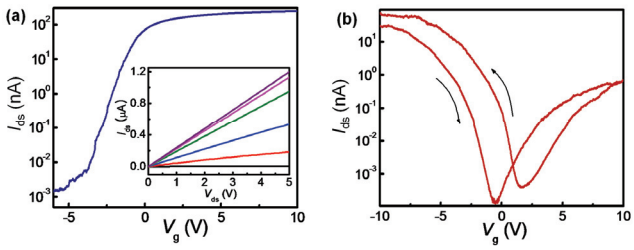
Fig, 2. (a) Histogram of the measured diameters of silicon nanowires grown at 620 °C. (inset) The average diameter vs. growth temperature.

On the other hand, single-crystal Ge nanowires grown by the similar growth method were tapered at increased temperature (Fig. 3). The morphology and growth direction of the Ge wires can be controlled by tuning growth conditions, such as temperature, pressure, and supply of vapor sources. We also observed the shape of Ge wires is strongly dependent on the growth direction of the wires. The difference in growth behaviors for Ge and Si nanowires seems attribute to surface oxidation of Si wires during the growth. It has been reported that a small amount of oxygen impurity is inevitable in conventional CVD systems and, unlike Ge nanowires, Si wires can be easily oxidized even at the very low oxygen pressure. The adsorption and accumulation of oxygen impurities on the side walls may assist the growth of uniform Si nanowires by the retardation of lateral growth, because the sticking coefficient of the precursors is extremely small on oxide surfaces at low supersaturation conditions.



Fig, 3. Proposed growth models and corresponding SEM images of metal-free (a) Si nanowires and (b) Ge nanowires.

We have easily implemented conductivity tuning by standard *in situ* phosphorus doping during the CVD growth, and we performed electrical transport measurements of field effect transistors (FETs) fabricated using the metal-free undoped and phosphorus-doped silicon nanowires. Figure 4a shows the current (I_{ds}) versus drain–source bias voltage (V_{ds}) curves for a phosphorus-doped silicon nanowire at different gate voltages (V_{gs}); the curves are typical of an *n*-channel silicon nanowire FET. On the other hand, an FET made of an undoped wire exhibited ambipolar characteristics (Fig. 4b), which displays the intrinsic nature of the undoped nanowire. Unintentionally doped Au-catalyzed Si nanowires frequently exhibit *p*-type behavior, which may attribute to their metal-induced deep-level defects, whereas none of our undoped Si nanowires exhibited p-type behaviors. We also measured zero-electric-field conductances from metal-free and Au-catalyzed silicon nanowires at various temperatures. The results suggested that metal impurities in Au-catalyzed wire might be strong scattering centers at low temperatures.



Fig, 4. Transfer characteristics (I_{ds}-V_{gs}) of a back-gated, phosphorus-doped *n*-type silicon nanowrie FET at V_{ds}=1. (inset of a) Current-voltage (I_{ds}-V_{ds}) characteristics for various V_{gs}. (b) Transfer characteristics (I_{ds}-V_{gs}) of a back-gated undoped intrinsic silicon nanowire FET at V_{ds}=3. The arrows show the sweep direction of V_{gs}.

3. Conclusions

Single-crystal silicon and germanium nanowires were synthesized by nucleation on nanocrystalline seeds and subsequent one-dimensional anisotropic growth without using external catalyst. Physical dimensions and electrical conductivities of the wires can controlled during the growth by adjusting process conditions. We also demonstrated high-performance FETs using our metal-free nanowires. This growth approach offers a method to eliminate potential metal catalyst contamination, and thus could serve as an important point for further developing nanowire nanoelectronic devices for applications.

Acknowledgements

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