Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1104-1105

Device and Circuit Co-Design Strategy for Radio Frequency (RF) Applications Based on Silicon Nanowire (SNW) MOSFETs

Seongjae Cho, Hee Sauk John, Il Han Park, Jung Hoon Lee, Hyungcheol Shin and Byung-Gook Park

Inter-university Semiconductor Research Center (ISRC) and
School of Electrical Engineering and Computer Science, Seoul National University
San 56-1, Sillim-dong, Gwanak-gu, Seoul 151-742, Republic of Korea
Tel: +82-2-880-7279, Fax: +82-2-882-4658, E-mail: avante@snu.ac.kr

1. Introduction

Silicon nanowire (SNW) metal-oxide-semiconductor field effect transistors (MOSFETs) have been under extensive researches recently for their merits such as immunity to short channel effects (SCEs), enhanced transconductance and scalability. Although there have been a number of researches on the characteristics and fabrication methods regarding a discrete device [1], applications of assembled SNW MOSFETs to radio frequency integrated circuit (RFIC) have been seldom reported. In this work, we have carried out a full-range approach, from device level to circuit level, for realizing an RF application based on 30-nm node SNW MOSFETs by device and circuit simulations: A 5.8 GHz low noise amplifier (LNA) adopting multi-fingered (MF) SNW MOSFETs has been designed and characterized, which shows improved noise figure (NF) of 3.1 dB and gain of 17.5 dB over the conventional LNA.

2. General Instructions

Fig. 1 shows the bird's eye view of the conventional planar (CPL) and SNW MOSFET devices constructed by ATLAS [2]. The physical gate lengths of the both devices are 30 nm and the SNW radius is 5 nm. The width of the CPL device is set to be 31.4 nm ($2\pi R = 31.4$ nm). The gate oxides are 3 nm thick, and the channel doping concentrations are 1×10^{15}/cm^3 for CPL and 2.5×10^{18}/cm^3 for SNW MOSFETs, respectively. To reduce the inferiority of CPL MOSFET, channel engineering has been performed: threshold voltage adjustment with 2×10^{18} B atoms/cm^3, punch-through stopper with 1×10^{17} B atoms/cm^3, lightly doped drain (LDD) of 5×10^{18} As atoms/cm^3 and deep S/D doping of 1×10^{20} As atoms/cm^3. The comparisons of transfer characteristics and primary parameters are shown in Fig. 2 and Table I.

MF structure is widely used in the analog/RF circuits to reduce the gate resistance. Fig. 3 shows the MF structures of CPL and SNW MOSFETs in 30-nm technology with 1P6M designed by Cadence [3]. Also, the schematic view of the circuits designed by HFSS [4], are shown in Fig. 4(a) and (b), where the number of fingers is 20 and the block unit width is 0.63 μm (=31.4 nm×20). For more realistic design, the parasitic components by wiring effects have been extracted by changing the node excitations systematically by HFSS and utilized, as illustrated in Fig. 5 and Table II. The maximum and current gains with frequency variation for the devices are depicted in Fig. 6. f_T and f_{max} of MF SNW MOSFETs are 215 GHz (43.3% increase) and 405 GHz (22.7% increase), which are superior to MF CPL block at an equivalent DC power consumption. To validate the extracted parameters, the simulated and the modeled s-parameters are compared in Fig. 7, which are in a good accordance within RMS errors of 2% up to 40 GHz.

Based on the realistic DC and AC parameters attained so far, a power-efficient 5.8 GHz LNA was designed and evaluated. Fig. 8 shows the fully integrated two-stage common source (CS) amplifier following 30-nm standard 1P6M CMOS process by ADS [5]. M1/M2 are commonly biased with 0.67 V and 0.51 V, in case of CPL and SNW MOSFETs, respectively, under an equivalent circuit power dissipation (2 mW). Also, a full shot noise model ($S_{id}=2qI_D$) has been considered in all the MOSFETs for more accurate prediction of performance [6]-[7]. Fig. 9 depicts the simulated S-parameters and NF of the LNAs. The NF and the gain (S_{21}) of SNW-based LNA are 3.1 dB at 5.8 GHz and 17.5 dB at input/output matching with the operation frequency, which is 14% lower and 16.7% higher than conventional LNA, respectively. Furthermore, the input/output return losses (S_{11}, S_{22}) are higher by 10 dB at the frequency of interest. Fig. 10 shows the Cadence layout of the LNA in Fig. 8, where the area is 1.5×0.93 mm^2. Table III compares the main RF performances of MF CPL and SNW MOSFET-based LNAs.

3. Conclusion

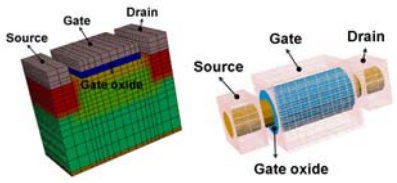
A 5.8 GHz LNA based on the MF SNW MOSFETs has been designed and characterized. It shows lower NF and higher power gain compared with the conventional LNA, which reveals great possibility that SNW MOSFETs can be also utilized in the RF applications of high performances.

Acknowledgements

We would like to acknowledge the research environment and the technical supports provided by Inter-university Semiconductor Research Center (ISRC) in Seoul National University.

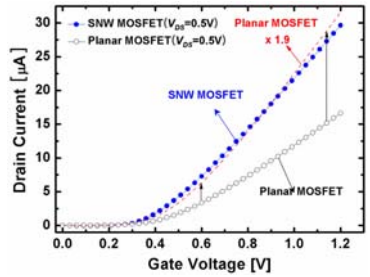
References

[1] J. Y. Song, *et al*., Jpn. J. Appl. Phys. **46** (2007) 2046.
[2] *ATLAS User's Manual*, Silvaco International (2008).
[3] http://www.seas.upenn.edu/~eecad/cadence/cadence.html
[4] *HFSS User's Guide*, ANSOFT Corp. (2005).
[5] *ADS 2006A*, Agilent Technology (2006).
[6] D. K. Shaeffer, *et al*., IEEE J. Solid-State Circuit. **40** (2005) 726.
[7] R. Navida, *et al*., J. Appl. Phys., **101** (2007) 124501.1.

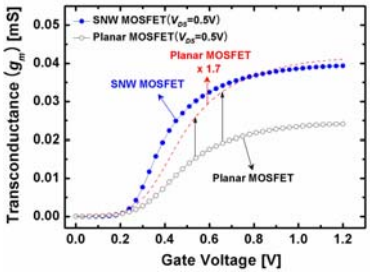


(a) (b)

Fig. 1. Schematic view of the devices in 3-D. (a) CPL (b) SNW MOSFETs.



(a)

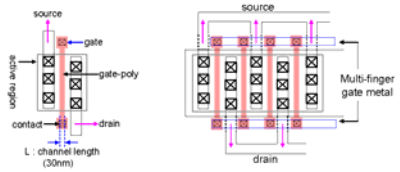


(b)

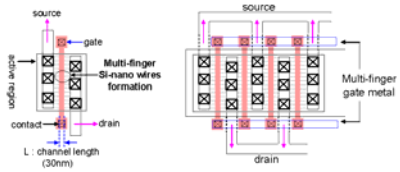
Fig. 2. Transfer characteristics. (a) on-state drain current (conductivity of SNW is higher by 1.9 times) (b) transconductance (1.4 times increase).

Table I Primary DC parameters of CPL and SNW MOSFETs.

	CPL	SNW
V_{TH} (V_{DS}=0.5V)	0.252 V	0.254 V
V_{TH} (V_{DS}=0.01V)	0.501 V	0.340 V
DIBL	506.8 mV/V	175.8 mV/V
SS (V_{DS}=0.5V)	158.4 mV/dec	66.1 mV/dec
$g_{m,max}$ (V_{DS}=0.5V)	0.0194 mS	0.0287 mS

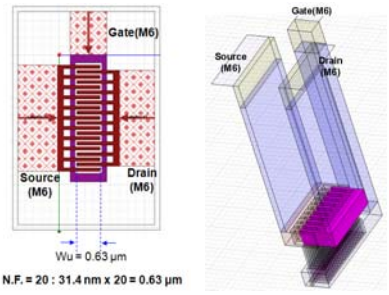


(a)



(b)

Fig. 3. Layout of MF structure based on (a) CPL and (b) SNW MOSFETs.



(a) (b)

Fig. 4. MF structure layout with M6 metal layers. (a) plane view (b) bird's eye view.

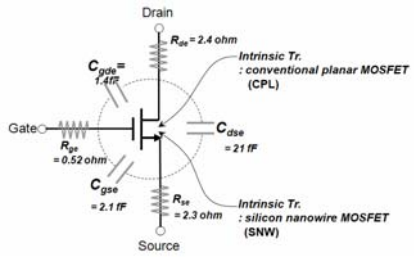
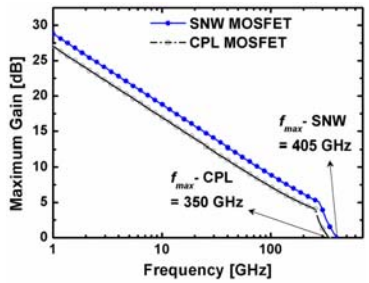


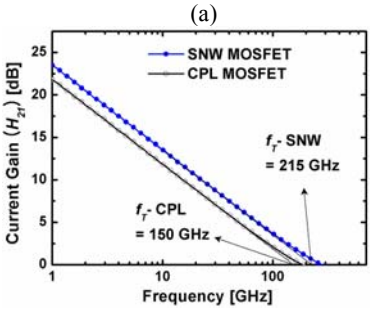
Fig. 5. Small-signal equivalent circuit model considering the wiring effects.

Table II Parasitic passive elements embdded in the small-signal modeling.

	Para	Unit	Value
Capacitance	C_{gde}	fF	1.4
	C_{gse}	fF	2.1
	C_{dse}	fF	21
Resistance	R_{ge}	Ohms	0.52
	R_{se}	Ohms	2.3
	R_{de}	Ohms	2.4



(a)



(b)

Fig. 6. High frequency characteristics. (a) maximum gain (MSG/MAG) (b) short-circuit current gain (H_{21}) of MF CPL/ SNW MOSFETs (V_{GS}=0.67 V, 0.51 V, respectively, at V_{DS}=0.5 V).

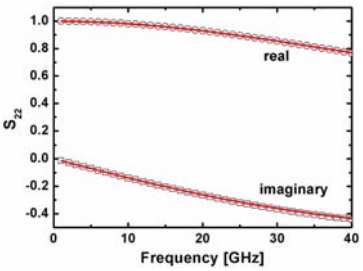


Fig. 7. Output reflectance coefficient (S-parameter at the output terminal).

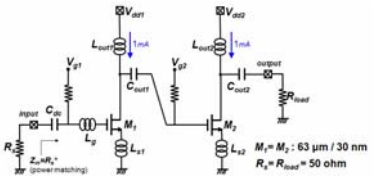
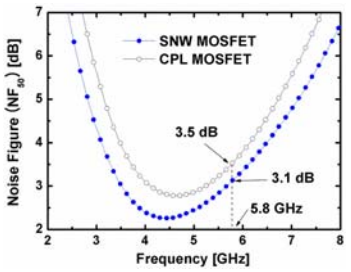
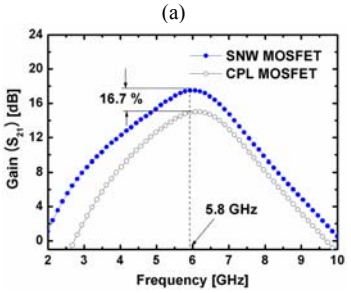


Fig. 8. Schematic diagram of the designed LNA based on CPL/SNW MOSFETs.

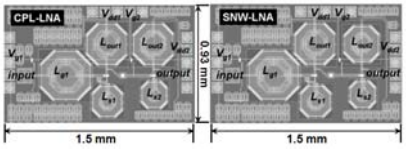


(a)



(b)

Fig. 9. S-parameters of the designed 5.8 GHz CMOS LNAs. (a) NF (b) peak forward gain.



(a) (b)

Fig. 10. Circuit layout (a) CPL and (b) SNW CMOS LNA (Area=1.5×0.93 mm^2).

Table III RF characteristics of LNAs.

Para	Gain	In. ref.	Out.ref.
	S_{21}	S_{11}	S_{22}
CPL	15 dB	< -20dB	< -20dB
SNW	17.5 dB	< -20dB	< -20dB
Para	Isolation	Noise Figure	
	S_{12}	NF50	
CPL	< -40 dB	3.5 dB	
SNW	< -40 dB	3.1 dB	