Performance Improvement of Poly-Si Nanowire Transistors Featuring In-Situ Doped Source/Drain

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1. Introduction

Poly-Si nanowire (NW) transistors have received considerable attention due to their promising potential in various applications [1][2]. Although the inherent granular properties of poly-Si render it much inferior to single-crystalline counterparts, the adoption of NW structure has been demonstrated to reduce this effect and results in CMOS comparable performance. The minimum subthreshold swing (SS) achieved nowadays is 79mV/dec [3]. However, the fabrication process includes sophisticated and low-throughput e-beam writing method. To lift this concern, we had previously proposed several innovative, sophisticated and low-throughput e-beam writing method. To lift this concern, we had previously proposed several innovative, sophisticated and low-throughput e-beam writing method. To lift this concern, we had previously proposed several innovative, sophisticated and low-throughput e-beam writing method. To lift this concern, we had previously proposed several innovative, sophisticated and low-throughput e-beam writing method. To lift this concern, we had previously proposed several innovative, sophisticated and low-throughput e-beam writing method.

2. Device Fabrication

The original fabrication process where S/D regions are accomplished by ion implantation is detailed in [6]. However, as is well known that S/D resistance play a significant role in total resistance for ultra-thin body devices, we employed in-situ doped S/D technique in this work to attain higher activation ratio and thus lower series resistance. Figure 1(a) and (b) depict schematically the top-view layout and the modified fabrication approach, respectively. This modified approach is very similar to the original one [6]: after solid-phase crystallization (SPC) step, without developing S/D photoreist patterns, rectangular NWs were directly formed by RIE inside the cavity (step (iv)). After hydrofluoric acid vapor clean, in-situ phosphorus doped poly-Si was then deposited (step (v)) followed by S/D region patterning (step (vii)). In this way, whole S/D regions were doped heavily and NWs retained their undoped characteristics as well. The following steps including 2nd gate stack deposition and patterning (step (vii)) as well as the standard metallization were all identical to the original approach. Control devices with implanted S/D were also fabricated for comparison.

3. Results and Discussion

Figure 2 displays the cross-sectional TEM image of a fabricated device, from which the rectangular NW channel can be observed. Transfer characteristics of the control device with ONO dielectrics are shown in Fig. 3. Here the operational denotation is briefly described: SG-1 and SG-2 mode denote the scheme when 1st or 2nd gate serves as the driving gate while the other gate electrode is grounded. In DG mode, both gates are connected together as the driving gate. Much steeper SS of 89mV/dec under DG mode than SG-1 and SG-2 modes is attributed to improved multi-gate controllability over NW channels, which is a consequence of volume inversion effect according to our previous study [6]. SS of DG mode is dramatically improved from 200mV/dec for devices with oxide as dielectric (data not shown) to 89mV/dec with ONO dielectric owing to additional passivation effect from the larger hydrogen content in the nitride film. The Ion/Ioff ratio is around 10⁸ for DG mode. As has been pointed out in [6], additional non-gated paths would have increased the series resistance for SG-1 mode. However, it can be observed that the device characterized in this study shows quite symmetric Id-Vg curve, implying that the non-gated paths related to the NW thickness is reduced and plasma damage induced during 1st gate lateral etching is lessened as well.

Transfer curves of the device with in-situ doped S/D are given in Fig. 4. The Ion/Ioff ratio is around 10⁸ for DG mode. Statistical analysis of Ion-Ioff plot comparison between implanted and in-situ doped S/D is shown in Fig. 5. The enhancement of Ion at fixed Ioff = 2 x 10⁻¹⁰ A is around 1.4X, which suggests the significance of S/D resistance for NG performance. Output curves of both devices are given in Fig. 6, again demonstrating much reduced series resistance from the steeper turn-on slope of in-situ doped S/D type. The reason for this improvement can be explained as follows: In the original fabrication process, S/D regions were formed by a low energy ion implantation such that dopants were situated near the top surface for the purpose of avoiding sacrificed gate controllability caused by inadvertent channel doping. Though this method attains good gate control over NW channels, it more or less leads to slight channel doping by the tail part of dopant distribution and is achieved at the expense of S/D resistance as only a small portion of S/D is heavily doped. On the other hand, in our modified approach featuring in-situ doped S/D, the activation ratio is intrinsically high than implanted counterpart and also whole S/D regions are heavily doped. Therefore, series resistance is significantly improved from 45kΩ to 8.1kΩ using linear regression method from the curves of Fig. 7.

Also noted from Fig. 4 is the enhancement of SS from 89 to 73mV/dec with DG operation when in-situ doped S/D is adopted. It can be ascribed to the elimination of unintentional doping of channel by ion implantation so that gate controllability is enhanced. To the best of our knowledge, this is the lowest SS achieved in the literature for poly-Si based devices.

4. Conclusion

In this study, by employing in-situ doped poly-Si as S/D, we demonstrate a high performance double-gated NW TFT with much reduced series resistance and SS as low as 73mV/dec. Throughout the whole fabrication process, no advanced lithography tools are required. Such NW devices with good switching properties show promising potential for reducing operation voltage and power consumption in practical applications.

Acknowledgment–The authors would like to thank the National Nano Device Laboratories (NLD) for assistance in device fabrication. This work was supported in part by the National Science Council of Taiwan under contract No. NSC 96-2221-E-009-212-MY3

References
Fig. 1 (a) Top-view and (b) schematic process flow of double-gated NW TFT with in-situ doped S/D.

Fig. 2 TEM image of the fabricated NW transistor.

Fig. 3 Transfer characteristics of the device with implanted S/D.

Fig. 4 Transfer characteristics of the device with in-situ doped S/D.

Fig. 5 Ion-Ioff characteristics of the NWTFT.

Fig. 6 Output characteristics of the NWTFT with different types of S/D.

Fig. 7 S/D series resistance extraction for NWTFT with (a) implanted and (b) in-situ doped S/D.