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Impact of adequate selection of channel direction on (001) and (110) wafer orientation for strained nanowire transistors

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1. Introduction

Nanowire transistor, promising alternative for planar bulk MOSFETs, has been studied intensively to implement in ultra high-performance ULSI and SoC due to their strong immunity against SCE and high drivability.[1-3] Introduction of strain technology to nanowire yields additional mobility enhancement but with a limited and incomplete under-pinning by a validated science knowledge-base. Building the science knowledge of transporting mechanism of nanowire with influence of strain in formats that is consistent with technology growth is very significant for implementing nanowire in the next generation ULSI technology. We have studied electrical characterization of strained nanowire FETs (s-nwFETs) to demonstrate impact of i) wafer orientation dependence using (001) and (110) plane and ii) adequate channel directions for transconductance enhancement based on and to reveal the carrier transport mechanism in nwFETs.

2. Experiments

We used *p*-type SOI wafers, (001) and (110) planes as substrates. The fabrication process is described elsewhere.[4,5] Figure 1 shows (a) the top-view schematic of fabricated strained nanowire transistor (s-nwFET), (b) (c) layouts of s-nwFETs, and (d) (e) (f) (g) the cross-sectional TEM images of each nanowire. Si nanowires are fabricated in (d) <100> direction on (110) plane, (e) <√2√21> direction on (110) plane, (f) <100> direction on (001) plane and (g) <110> direction on (001) plane. Scale bar denotes 50nm. The channel lengths are 2, 3, and 5μm, and nanowire lithography width (W_l) is 80~500nm.

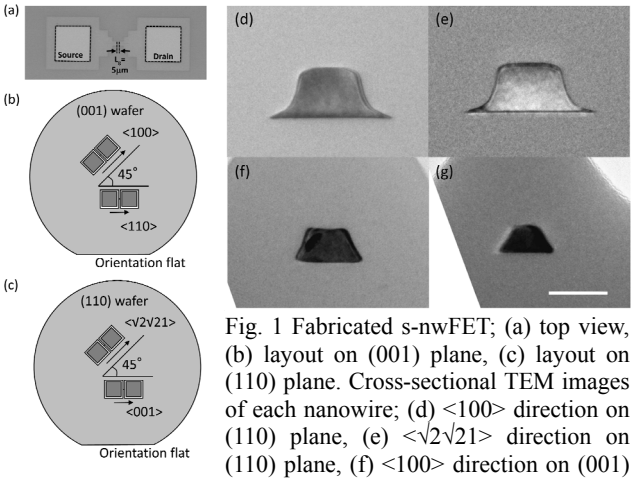

Fig. 1 Fabricated s-nwFET; (a) top view, (b) layout on (001) plane, (c) layout on (110) plane. Cross-sectional TEM images of each nanowire; (d) <100> direction on (110) plane, (e) <√2√21> direction on (110) plane, (f) <100> direction on (001) plane, and (g) <110> direction on (001) plane. Scale bar denotes 50nm.

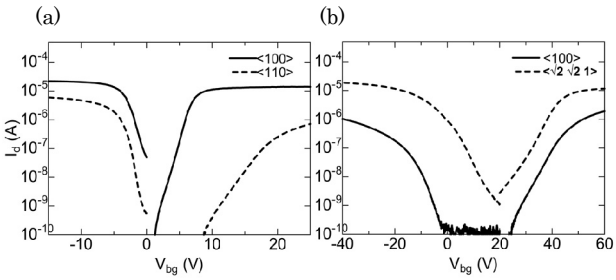

Fig. 2 I_{ds}-V_{bg} curves for (a) (001) plane and (b) (110) plane. Solid lines denote <100> direction for both plane, and dashed lines denotes <110> direction for (001) plane and <√2√21> direction for (110) plane.

3. Results and Discussion

I-V measurement is carried out for electrical characterization of s-nwFETs, with the backgate voltage (V_{bg}) applied to the *p* substrate. Figure 2 shows I_{ds}-V_{bg} curves for both (001) and (110) planes. Subthreshold slopes for *n*-type and *p*-type <100> direction nwFETs are 3180mV/dec, 2860mV/dec on (001) plane, and 568mV/dec and 650mV/dec on (110) plane. Devices on (001) plane shows improved subthreshold slopes.

The conduction and valance band energy of s-nwFETs are evaluated by *T-CAD* tool, and the simulation results are shown in figure 3 for (a) (001) plane and (b) (110) plane. Device profiles are recreated from the cross-sectional TEM images as shown in fig.1. V_{bg} is set at 10V, and V_d is set at 0.1V. Band vending is consistent among both devices even the nanowire cross-sectional profiles are different (fig. 1). Electrical potentials are also calculated, and they are also consistent (not shown in this paper).

Transconductance (g_m), the slope of I_{ds}-V_{bg} curves in

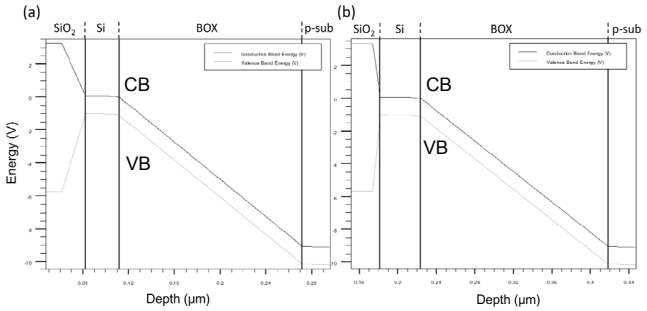

Fig. 3 Simulation results. Conduction band (CB) energy (solid line) and valence band (VB) energy (gray line) against (a) (001) plane and (b) (110) plane s-nwFETs.

the linear region, $g_m \equiv (\partial I_{ds}/\partial V_{bg}) = (W/L_g)(\varepsilon/t_{OX})\mu V_{ds}$, is normalized by W and t_{OX}, determined from the cross-sectional TEM images of nanowires (fig. 1) and the defined value of the gate length (L_g) to give $g_m^* = g_m(L_g/W)t_{OX} = \mu\varepsilon V_{ds}$.

Figure 4 shows g_m^* for (a) *n*-type and (b) *p*-type s-nwFETs with channel direction and wafer orientation of <110> direction on (001), <100> direction on (001), <100> direction on (110) and <√2√21> direction on (110). Solid circles denote raw data for each condition, gray circles denote g_m^* with L_g=2μm, and open circles denote g_m^* with L_g=3,5μm. For *n*-type, the device with <100> channel on (001) yields the highest g_m enhancement, and for *p*-type, that with <100> channel on (110) yields the highest enhancement. g_m^* with L_g=2μm shows the highest values in all conditions. This indicates the strong dependence of g_m^* on L_g, since the g_m is normalized by L_g to yield g_m^*.

Figure 5 shows g_m^* for (a) *n*-type and (b) *p*-type <100> direction strained nwFETs. Solid circles denote g_m^* for (001) plane, and open squares denote g_m^* for (110) plane. Big solid circles and big open squares with solid lines denote average values for each condition. For *n*-type, g_m^* is enhanced in (001) plane compared to (110) plane. The average value of g_m^* for (001) plane at L_g=2μm, for example, is improved by a factor of 2.2. This is due to the lighter effective mass of electron on (001) plane than (110) plane

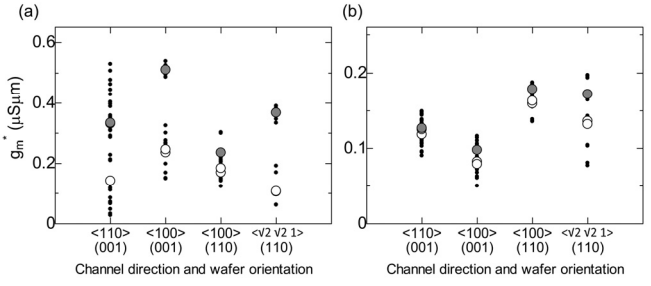

Fig. 4 g_m^* for (a) *n*-type and (b) *p*-type strained nwFETs. Closed circle denote g_m^* for each channel direction and wafer plane. Gray circles in bigger size denote the average values of g_m^* with L_g=2μm, and open circle in bigger size denote the average values of g_m^* with L_g=3,5μm

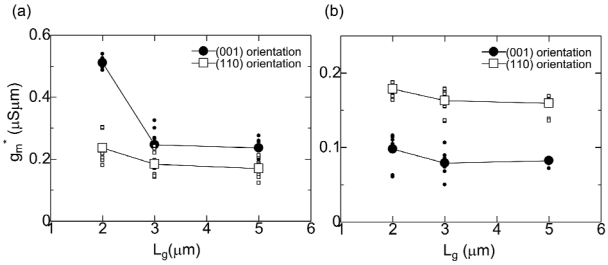

Fig. 5 g_m^* for (a) *n*-type and (b) *p*-type <100> direction s-nwFETs. Circles denote (001) plane and squares denote (110) orientation. Bigger circles and squares with solid lines denote average values for each condition.

in <100> direction.[7] For *p*-type, on the contrary, g_m^* is enhanced in (110) plane compared to (001) plane. The average value of g_m^* for (110) at L_g=2μm is enhanced by a factor of 1.8 compared to (001) plane. This is due the anisotropy of effective mass of holes.[8] Though g_m^* is normalized by L_g, it has L_g dependence. Fig. 5 clearly shows the dependence of g_m^* on L_g. This enhancement may be due to less contribution of phonon scattering because the channel length is approaching to the average mean free path of phonon, which is 300nm at room temperature.[9]

4. Conclusions

Enhanced transconductance in s-nwFETs is demonstrated with adequate combination of channel direction and wafer plane. g_m^* for *n*-type s-nwFETs is enhanced by a factor of 2.2 with <100> direction channel on (001) plane, and that for *p*-type is enhanced by a factor of 1.8 with <100> direction channel on (110) plane. This is due to the lighter effective mass of carriers along the selected direction on the adequate wafer plane.

Acknowledgements

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