Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1120-1121

Electric characterization of carbon nanotubes grown at low temperature by remote plasma chemical vapor deposition for LSI interconnects

Masatomo Iizuka[1], Daisuke Yokoyama[1], Kentaro Ishimaru[1], Isamu Yuitho[2], Teruaki Takeuchi[2], Shintaro Sato[3], Mizuhisa Nihei[3], Yuji Awano[3] and Hiroshi Kawarada[1]

[1]Waseda Univ., School of Sci & Eng.
3-4-1, Ohkubo, Shinjyuku-ku, Tokyo 169-8555, Japan
Phone: +81-3-5286-3391 E-mail: kawarada@waseda.jp
[2]Nanotechnology Research Center, Waseda University
513, Waseda Tsurumakityou, Sinjuku-ku, Tokyo 162-0041, Japan
[3]MIRAI-Selete (Semiconductor Leading Edge Technologies, Inc.)
10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan

1. Introduction

Carbon nanotube (CNT) is one of promising materials for future LSI interconnects because of its unique properties such as high current density exceeding 10^9 A/cm^2, high thermal conductivity and ballistic transport. For interconnect application, it is essential to synthesize densely-packed CNT-bundles at a low temperature below 400˚C. We have grown multi-walled carbon nanotubes (MWCNTs) in vias (2μm) with remote plasma CVD, and measured their electric properties [1]. However the resistance of the CNTs grown in smaller vias are needed to be evaluated because actual via sizes in LSI are smaller than we made. In this study, we fabricated fine vias (<500 nm) made of MWCNTs, and characterized their properties by 4 probe mesurment.

2. Experimental

We fabricated CNT vias shown in Figure 1. Bottom electrodes are composed of Cu wiring (300 nm) covered by Ta barrier layer (20 nm). After depositing a tetraethylorthosilicate (TEOS) dielectric layer (200 nm), via holes were made using electric beam lithography and Inductive Coupled Plasma-Reactive Ion Etching (ICP-RIE) dry etching. The size of via holes ranges from 200 to 500 nm. TiN layer and Co catalyst particles were formed over the whole substrate after fabrication of via holes. The Co catalyst particles for CNT growth were size-classified using impactor [2] and they were deposited on TiN layer with the average diameter of 3.8 nm.

For CNTs growth, we used the remote plasma CVD equipment with an antenna and the spherical plasma is at the edge of the antenna generated by microwave (2.45 GHz). The source gas for CNT growth was a mixture of H_2 and CH_4 at 20 Torr and the microwave power was 60 W. Although our method uses plasma, there is less damage to sample on the substrate than conventional plasma CVD equipments because the plasma is fixed to the antenna edge and the substrate holder is located 50 mm away from the discharging area. When we grounded the antenna and applied negative bias voltage to the substrate, no distinct current was measured. Therefore, there are no ions, which affect the CNTs growth, around the substrate and only radicals contribute to CNTs growth. Furthermore, the growth temperature depends on only the heater, which indicates that our equipment is suitable for low temperature growth of CNTs. The growth temperature of CNT-bundles was 390˚C under the allowing temperature of 400˚C in Si LSI process.

Then, CNTs were held by spin on glass and flattened with chemical mechanical polishing (CMP) to use inner shell conductions[1]. To measure electrical properties, Ti contact layer (10 nm), Cu wiring (300 nm) and Ti layer were deposited as the top electrodes. Via resistances were measured with 4 probe method at room temperature.

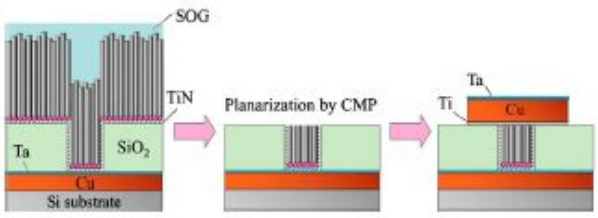

Fig. 1 The structure of CNT via for electrical properties

3. Result and Discussion

Figure 2 shows SEM images of vias shaved and filled with CNTs before and after CMP. It is confirmed that CNTs are finely shaved without fault. CNTs grow equally in all holes with good reproducibility. The diameter of grown CNTs ranges 5 to 10 nm (avg. 7 nm)and the density of CNT is 4.0×10^{11} cm^{-2} . As shown in Figure 2, vertically aligned CNTs grow densely. The TEM image shown in Fig.3 indicates that a CNT grown at the low temperature of 390˚C maintains a hollow structure, having a good quality of graphite sheets enough to realize the carrier conduction.

Figure 4 shows good ohmic behaviour between CNTs and electrodes. The measured via resistance of 12 Ω at ϕ200nm via, 3.7 Ω at ϕ350nm via and 3.0 Ω at ϕ500nm via .

Then, we introduce “normalized resistance” defined as below formula.

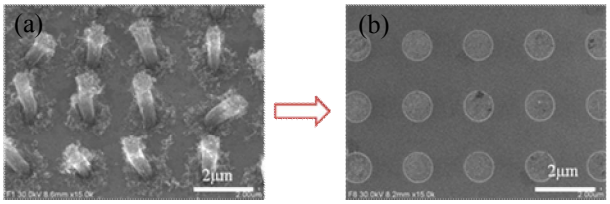

Fig. 2 SEM images of CNT vias .(a)Before CMP. (b)After CMP.

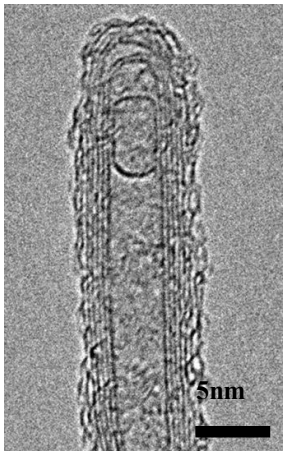

Fig 3. High magnification TEM image of CNT grown at 390°C.

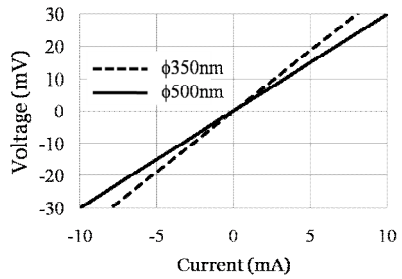

Fig 4. I-V characteristics of CNT vias

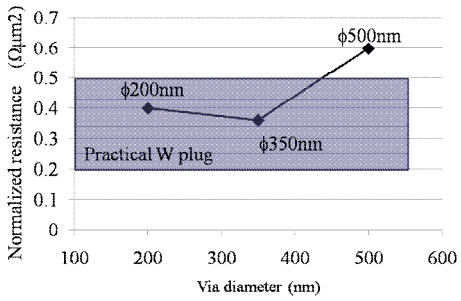

Fig 5. Via diameter – Normalized resistance

$$Rs = R \cdot S = \rho \cdot l \qquad (1)$$

In this formula, Rs shows normalized resistance, R is via resistance, S is surface area, ρ is resistivity, l is via length. The reason why we don't use resistivity but normalized resistance is that CNT vias are normalized only surface area if CNTs show ballistic conductance. Figure 5 shows the value of normalized resistance for each via sizes. When via sizes decrease, the normalized resistances roughly keep their value. This shows CNTs in via keep their quality regardless of decreasing via size. The lowest value of normalized resistance is 3.6×10^{-1} Ωμm^2 which is equivalent to practical W plug, and comparison with quantum resistance (6.45 kΩ / tube), four inner layer of CNTs are used as conduction passes.

Figure 6 shows (a) Atomic Force Microscope (AFM) image and (b) current mapping image of same CNT vias. By visualization of current, it is confirmed that only the via area guarantees electric current and good contacts between CNTs and bottom electrodes, because in current mapping current conduct same position of vias in AFM image and is finely shown. By using current mapping, we confirmed current only in via holes and good contact between CNTs and bottom electrode.

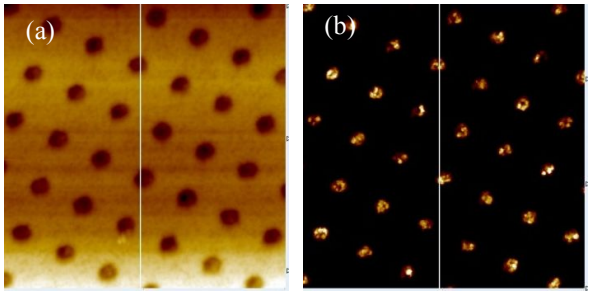

Fig 6. (a) AFM image of CNT vias. (b) Current mapping image of CNT vias.

4. Conclusion

We fabricated CNT-via grown at a low temperature of 390°C using remote plasma CVD and succeeded in measuring electrical properties of CNTs by achieving ohmic contacts. The lowest normalized resistance of via is equivalent to that of practical W plug. By cutting caps of CNTs with CMP, CNT 4 inner shell conductions are realized.

Acknowledgements

This work was partly completed as part of the MIRAI Project supported by NEDO.

References

[1] D. Yokoyama, T.Iwasaki, Tsuyoshi Yoshida, Shintaro Sato, Takashi Hyakushima, Mizuhisa Nihei,H. Kawarada, et al., Appl. Phys. Lett. 91, 263101(2007)

[2] S. Sato, M. Nihei, A. Mimura, A. Kawabata, D. Kondo, H. Shioya, T. Iwai, M. Mishima, M. Ohfuti and Y. Awano, Proc. IEEE Int. Tech. Conf. 2006 (2006) 230