

Identification of Single Boron Acceptors in Nanowire MOSFETs

A Base for Single-Dopant Electronics

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1. Introduction

Highly scaled MOSFETs suffer serious problems from the fluctuation of the dopant-atom number [1], but in turn offer a new concept of a device in which the operation is regulated by means of individual dopant atoms [2-4]. These issues have stimulated recent research interest [5-12] in the detection of single dopants in silicon. Here, we report our recent work [8-12] on the identification of the position of single dopants in nanowire MOSFETs, which is a base for the realization of the so-called *single-dopant electronics*.

2. Device Structure for Single-Dopant Detection

We fabricated nanowire *p*MOSFETs on an SOI substrate, which comprises a 32-nm-thick boron-doped Si wire, a p^+ source/drain, and a two-layer (front and upper) poly-Si gate (Fig. 1). The front gate controls the electrical potential of a small wire region underneath it, while the upper gate, with a negative voltage, creates a hole accumulation layer acting as leads for the front-gate nanowire MOSFET. Owing to this two-layer gate, the channel under the front gate is separated from the heavily doped source/drain, making it possible to investigate the effect of the low-concentration channel dopants without the annoyance of dopant diffusion from the source/drain. We prepared MOSFETs with four doping concentration: undoped, 0.2, 0.9, and $5.0 \times 10^{17} \text{ cm}^{-3}$, which correspond to the mean boron atom number n_A of 0, 1, 5, and 26, respectively, under a front gate with a 40-nm width and 40-nm length.

3. Results

The MOSFET conductance G was measured as a function of the front gate voltage (V_F) with a constant upper gate voltage (V_U) using either the backgate voltage (V_B) or source-drain voltage (V_L or V_R) as parameters at temperature of 6 or 26 K.

3-1. Detection of Single Boron Acceptors [8]

Figure 2 shows how the conductance characteristics change with n_A . With reference to the undoped sample, which exhibits 'clean' characteristics (bottom right panel in Fig. 2), the doped ones show conductance modulation in the subthreshold region. For samples with $n_A = 1$, only one series of modulation humps is observed in the subthreshold region (two top panels). We ascribe these humps to the capture of holes by a single boron acceptor. It should also be noted that the *pattern*, or the V_{BG} dependence of the conductance level of the hump differs from one sample to another. This difference provides information on the depth of the associated acceptors as we will explain with Fig. 3. As n_A increases, the structure becomes complicated. For $n_A = 5$ (two middle panels), we can still recognize the regulated pattern, which exhibits a mixture of that for single-dopant cases (two top panels). However, for $n_A = 26$, such a pattern was lost. This is consistent with our previous results for macroscopic transport of doped MOSFETs [10,12], where, with this highest doping concentration, hopping predominated in the current and the conduction path changed in a complicated manner as V_B changed.

3-2. Identification of the Depth Position [9]

Depth position, i.e., how far single dopants are located from the SiO_2/Si interfaces, can be qualitatively obtained from a detailed analysis of the conductance data on the V_F - V_B plane. This is because, using V_B as a parameter, we can control the depth of the MOSFET channel (see top left of Fig. 3) and thus voltage conditions for single dopants to capture a hole. Figure 3(a) shows the data for an undoped sample, where $d\text{Log}G/dV_F$ is plotted to accentuate the subthreshold region represented as a black belt. As shown in Figs. 3(b)-(d), the humps observed in Fig. 2 are seen as white curves and their slopes are different from one to another. The acceptor in Fig. 3(b) was assigned as one located near the front interface because the slope (dV_F/dV_B) of the white curve became gentler when the back channel opened. This behavior is explained by the shielding of the electrical flux by the back channel. In a similar manner, the acceptor in Fig. 3(c) was assigned as one located around the middle of the SOI. The MOSFET in Fig. 3(d) contains two acceptors, one near the back interface and the other around the middle of the SOI. A capacitive coupling between the two acceptors was successfully observed as indicated by a white circle in Fig. 3(d).

3-3. Identification of the Horizontal Position: Impact of Source-side Dopants on MOSFET Subthreshold [11]

Identifying dopant position along the transport channel is of greater importance because it is expected that dopants near the source (emitter) terminal would have the biggest impact on the subthreshold nature of the MOSFET. Figure 4 shows $d\text{Log} g/dV_F$ for a single dopant sample, where g is the differential conductance. Top left and bottom left figures show data taken at $V_L = 0$ and $V_R = 0$, respectively. Comparing them, we see that conductance modulation, seen as white lines (also indicated by thin black arrows), has different slopes. That is, the modulation pattern is asymmetric in terms of the flipping of the terminal grounded. The acceptor is thus assigned to be located near the end of the channel, near the right terminal in the present case. Noteworthy is that the shift of the characteristics is always larger when the acceptor is located near the source (emitter) than when it is located near the drain (collector). For example, as shown in the right half of Fig. 4, the amount of the shift is larger when $V_R > 0$ (holes emit from the right terminal) than when $V_R < 0$ (holes emit from the left terminal). This is a proof, *on the level of single dopants*, that dopants near the source significantly affect the subthreshold nature of the MOSFET.

4. Summary

We have identified the location of single boron acceptors in nanowire MOSFETs. With the help of computer simulation of the potential profile, methods for identifying location more precisely and for counting the dopant-atom number will be developed.

Acknowledgment

This work was partly supported by JSPS KAKENHI (20241036).

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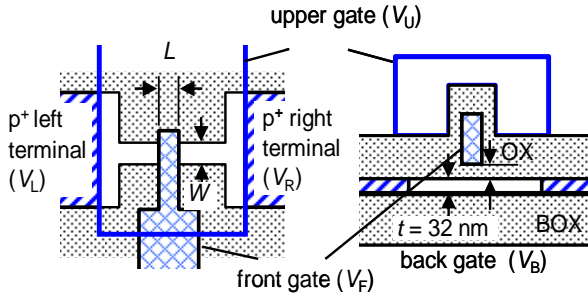


Fig. 1: Top- and cross-sectional views of the nanowire MOSFETs fabricated on a (100) SOI substrate. The SOI is 32-nm thick and the front-gate channel is 40-nm long and 40-nm or 70-nm wide. OX (35-nm thick) and BOX (400-nm thick) stand for gate oxide and buried oxide, respectively.

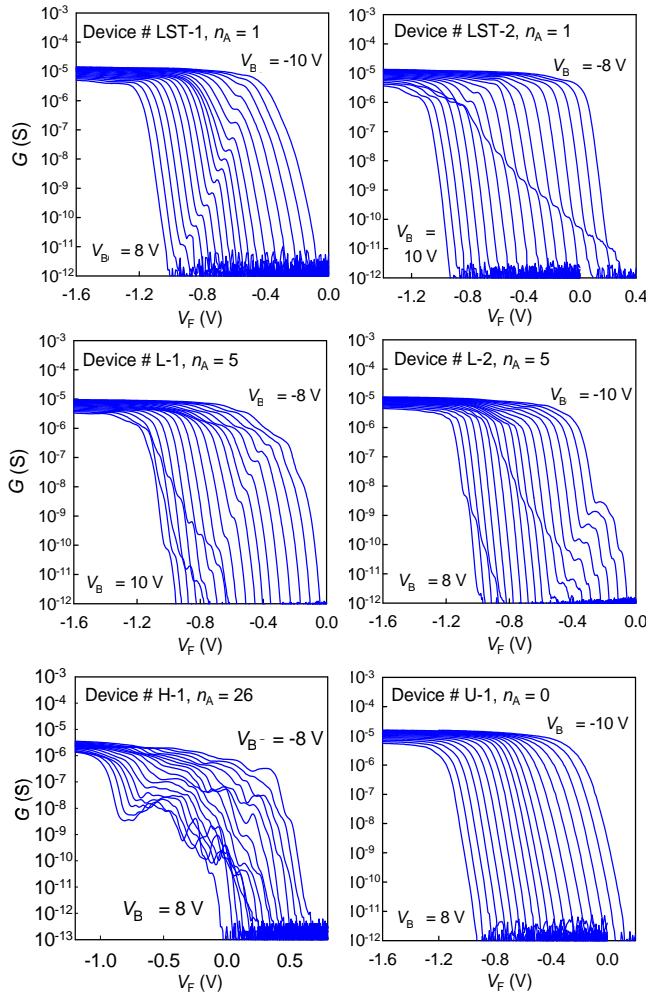


Fig. 2: Examples of conductance characteristics of nanowire MOSFETs with the mean boron number $n_A = 1$ (top), 5 (middle), 26 (bottom left), and 0 (undoped; bottom right), measured at 26 K. The V_U was fixed at -5 V and V_{BG} was changed in 1-V steps. The source-drain voltage was 10 mV.

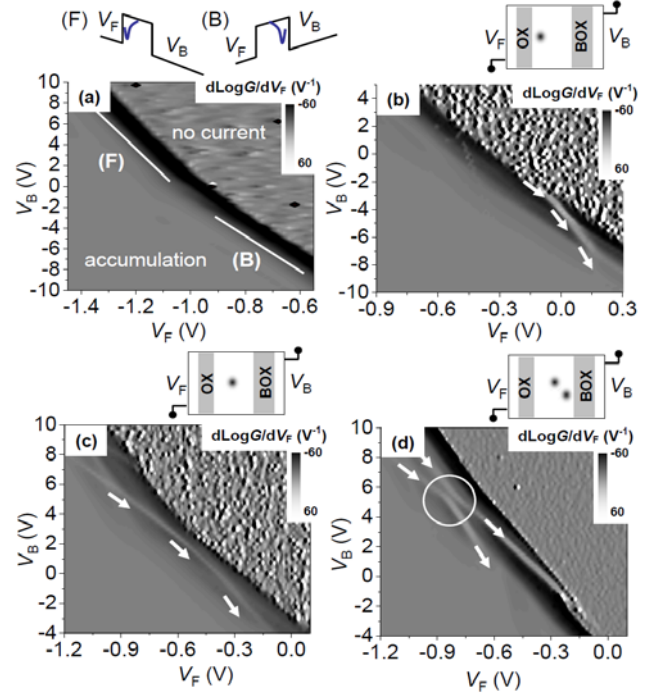


Fig. 3: $d\text{Log}G/dV_F$ in the V_F - V_B plane for undoped (a) and three different samples (b)-(d) with $n_A = 1$ -2, measured at 6 K. In (a), white lines (F) and (B) show the threshold voltage lines for the front and back channels respectively. Top of (a) illustrates the potential diagrams around the valence band edge when the front and the back channels open. In (b)-(d), the arrows are guides of the modulation curves. The depth of the acceptors is schematically shown in each figure, where the acceptors are represented by dots. In (d), the circle indicates a region where coupling of two acceptors is observed.

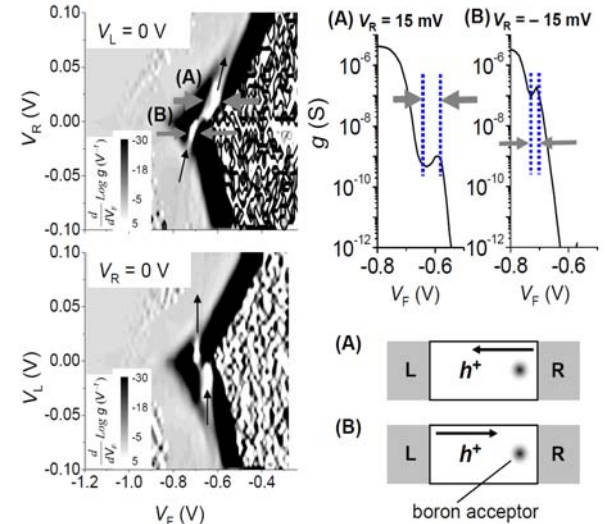


Fig. 4: $d\text{Log} g/dV_F$ in V_F - V_R (top left) and in V_F - V_L (bottom left) planes for a sample with a single boron acceptor, measured at 6 K. The top right shows the g vs. V_F curves for a fixed V_R . The amount of the shift indicated by horizontal gray arrows is larger when holes emit from the right terminal, i.e., for (A). The bottom right illustrations indicate the direction of the hole current and the location of the acceptor for (A) and (B).