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Electric double layer gate FETs based on silicon

Takashi Yanase[1], Toshihiro Shimada[1] and Tetsuya Hasegawa[1,2]

[1]Department of Chemistry, The University of Tokyo
Bunkyo-ku, Tokyo 113-0033, Japan
Phone: +81-3-5841-7595 E-mail: shimada@chem.s.u-tokyo.ac.jp
[2]CREST-JST, 4-1-8 Honmachi, Kawaguchi, Saitama 331-0012, Japan

1. Introduction

Considerable research activities are focused to realize electronic circuits on flexible film substrates. Organic semiconductors are one of the potential candidates of the active materials for the flexible circuits due to their mechanically plastic, low-weight and printable nature. However, the gate voltages required for metal- insulator- semiconductor field effect transistor (MIS-FET) operation is very high -- usually almost reaching to 100V -- due to the difficulties in fabrication of stable ultrathin insulators and to the low carrier mobility of organic semiconductors. The gate voltage should be reduced to the order of 1V for daily and/or wearable applications. One approach to solve this problem might be to use electric double layer (EDL) as the gate insulator [1,2]. EDLs are formed near the electrode/electrolyte solution interfaces by applying voltage. When a voltage is applied, ions in the electrolyte solutions move toward both electrodes, resulting in the formation of Helmholtz plane. The Helmholtz plane and the electrode surface have opposite charges, forming a kind of capacitors called electric double layer. The distance between Helmholtz layer and the electrode surface is quite small, approximately 1 nm, therefore capacitance of electric double layer becomes great. If EDL is used as a gate capacitor in FETs instead of gate oxide, large amount of carriers can be accumulated with small gate voltage.

The concept of EDL-gated FETs (EDL-FETs) is applied to organic semiconductors [1,2] and oxide semiconductors [3]. However, the main focuses of the studies are rather on fundamental physics, such as to seek the highest mobility or achieving metal-insulator transitions. Aspects determining practical device performance of EDL-FET, such as pulse response or frequency dependence of the FET characteristics, have not been studied in detail.

The purpose of the present study is to clarify the dynamic properties of EDL-FETs by using silicon as a model semiconductor. It is considered that the properties of silicon are well known so that it is easy to investigate properties of electrolyte solutions as gate of FETs. For example, it is expected that ion dynamics in EDL will be probed by pulse or AC response of the EDL-FET. Since the dynamic FET response reflects the carrier density and the mobility in semiconductor electrode in the vicinity of EDL, it might give the information different from the macroscopic capacitance measurements [2].

2. Experiments

We fabricated electric double layer FETs based on Si substrate and measured I-V characteristic. Figure 1 shows the structure of FETs. High resistivity (1000 Ωcm - 3000 Ωcm) Si wafer (thickness 300 μm) was used to fabricate FETs. Si substrates cut into 15mm x 15mm and were cleaned by RCA cleaning method and native oxide layer was removed by diluted HF solution. Aluminum source and drain electrodes were vacuum deposited as soon as possible after removal of native oxide. A glass cylinder with the size of 6mm inner diameter was glued on the substrate using epoxy resin to include the active region between the source and the drain electrodes. Then the electrolyte liquid was filled in the cylinder. The liquid was $LiBF_4$ dissolved in polyethyleneglycol (PEG) or an ionic liquid. The mixing ratios of BF_4Li/polyethyleneglycol (PEG) in the electrolyte solutions were [Li]: [O] =1 : 679 and 1 : 98. The ionic solution is 1-ethyl-3-methylimidazoliumtetrafluoroborate. Finally, platinum gate electrode was immersed in the gate liquid.

In order to clarify the frequency dependence of the EDL-FET, two kinds of measurements were performed. The first one was capacitance measurement using different frequencies. In this measurement, gold electrode with a known area was prepared on glass substrate and the capacitance was measured using the same platinum electrode used for the FET measurements. The second measurement was on the pulse response of EDL-FET using a specially designed circuit.

3. Results and Discussions

Figure 2 shows the FET characteristics of an EDL-FET using $LiBF_4$ / PEG as the electrolyte. The gate leakage current was negligible compared with the drain current when the gate and drain voltage was within the plotted range. The device characteristics shown in Fig. 2 were completely repeatable. However, it was found that substantial gate leakage current was observed when the gate and / or drain voltage was high and the FET characteristics was irreversibly lost. It shows the occurrence of electrochemical reaction on silicon or source/drain electrodes.

It can be seen that the drain current is sub-mA at the drain voltage of 0.5V, which is much larger than the ordinary organic semiconductor FETs. The mobility can be estimated from the gate capacitance values using same electrolyte. Although the effects of carrier diffusion and incomplete sealing outside the channeling region must be considered for the precise estimation of the mobility, it was derived as ~ 100 cm^2/Vs from a rough analysis.

This device is characterized by low on/off ratio, which was approximately 6. The reason is probably the bulk conduction of silicon. Although we used a silicon wafer with high resistivity, the thickness of the silicon wafer is enough to account for the high off current of the device.

When we used more highly doped silicon wafer as the active material, it almost did not respond to the gate bias. In order to increase the on/off ratio, fabrication of thin or narrow crystals or inversion doping should be considered.

Figure 3 shows the frequency dependence of the capacitance. Electrolyte solution of PEG shows steep decrease of the capacitance as a function of frequency, whereas the ionic liquid retains relatively high capacitance at high frequencies. These characteristics agrees well with the previous report[] but the microscopic explanation is not given so far. We will compare the pulse / AC response of the silicon EDL-FET to see what determines this frequency dependence.

4. Conclusion

We fabricated EDL-FETs using semi-insulating silicon single crystal wafer as the active materials in order to study the ion dynamics in electrolyte liquid. The measured characteristics showed FET performance and the carrier mobility was nominally very high. The on/off ratio was ~6 and was determined by bulk conduction in silicon. The pulse response was measured to study the ion dynamics in the vicinity of the semiconductor electrode.

References

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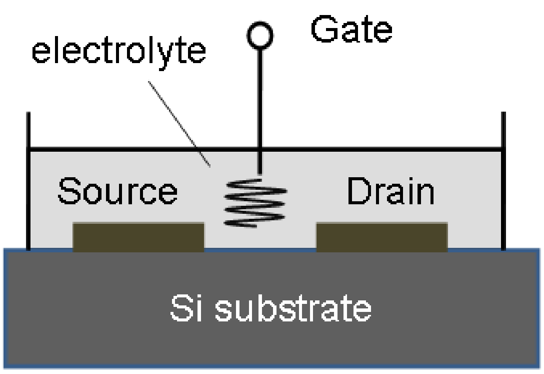

Fig. 1 Structure of the measured device

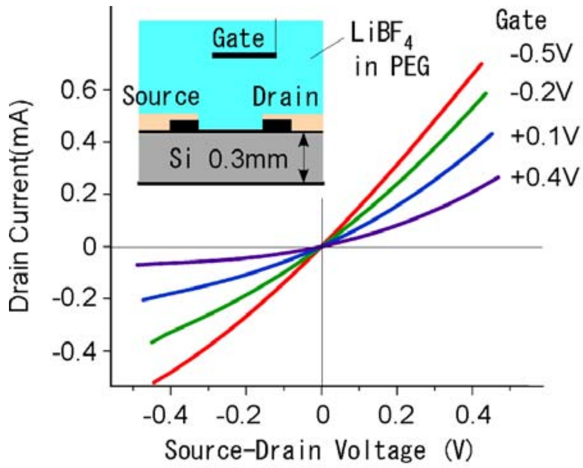

Fig. 2 FET characteristics of a silicon EDL-FET.

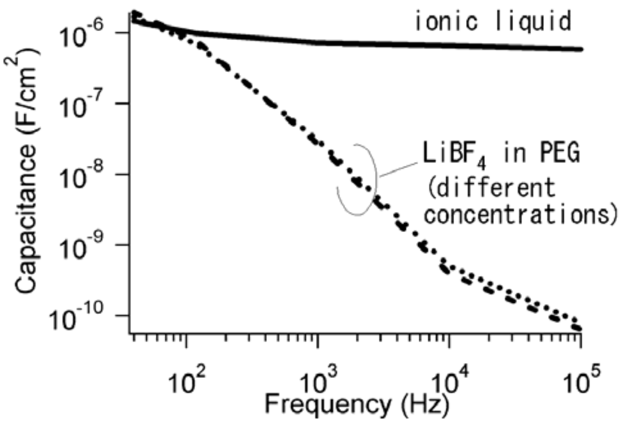

Fig. 3 Capacitance-Frequency plot of electrolytes