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Organic inverters with double-gate organic thin-film transistor using photosensitive polymer as the dielectric layer

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1. Introduction

For the application of organic thin-film transistors (OTFTs) to a wide variety of low-cost device components, including logic circuit elements, the principal objective of materials development is to maximize the carrier mobility. Throughout this progress, despite proposed new geometries, such as vertical channel OTFTs [1], the standard planar deices remained basically unchanged, with TFT structures, implemented in bottom gate (BG) or top gate (TG), as the most common configurations. Double-gate transistors have been developed as an industrially important technology to reduce the size of the transistors in integrated circuits.

2. General Instructions

Pentacene OTFTs with double-gate (DG) structure fabricated in our study is shown in Figure 1. The glass substrate with the Indium-tin-oxide (ITO) pattern was cleaned with acetone, isoprophyl alcohol, methanol, and de-ionized water in sequence to remove residual impurities in an ultrasonicator. ITO on a glass substrate, etched by photo-lithography, was used as a bottom gate electrode (G1). For forming the ammonium dichromate polyvinyl alcohol (DCPVA) dielectric layer, first PVA was dissolved in deionized water and ammonium dichromate as photo-sensitizer was incrementally added to the solution. The PVA solution was prepared with an ammonium dichromate concentration of 4 wt% of the PVA concentration. The substrate was coated with photopolymerizable blend and then dried under vacuum for a photolithographic process. The thickness of the DCPVA layer was 600nm. In order to induce the photo cross-linking, the photoirradiation was exposed on the DCPVA layer at 365nm (exposed light energy, 240 mJ/cm^2) cured gate dielectric. The exposed DCPVA was developed in deionized water for isolating each OTFT and forming the vias to connect the bottom gate (G1) to the top gate (G2).

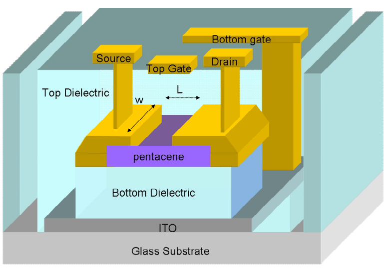

Figure 1 Pentacene OTFTs with double-gate (DG) structure

Pentacene active layer purchased from Aldrich was grown on the DCPVA layer by thermally evaporation [2, 3] and the thickness of the active layer was about 500 nm at the rate of 0.5Å/sec. The source electrode and the drain electrode were prepared on the pentacene layer using a 100nm Au layer. The channel length, L and width, W were defined as 50 and 200 μm, respectively.

As a passivation layer, DCPVA was selected. To protect pentacene active layer from the organic solvent such as PGMEA, DCPVA was proposed. PVA is water-soluble and the damage to the pentacene active layer can be minimized compared with other materials dissolved in organic solvents. On top of the pentacene layer, a 600 nm thick DCPVA film was spin-coated. In order to pattern the circuit line of the source and drain electrode, the photoirradiation was exposed on the DCPVA layer. On the developed DCPVA with deionized water dried under vacuum, a 100 nm thick Au film was thermally deposited to form a top-gate electrode (G2) and to connect the circuits of the source and drain electrode to form a D-inverter as Figure 2.

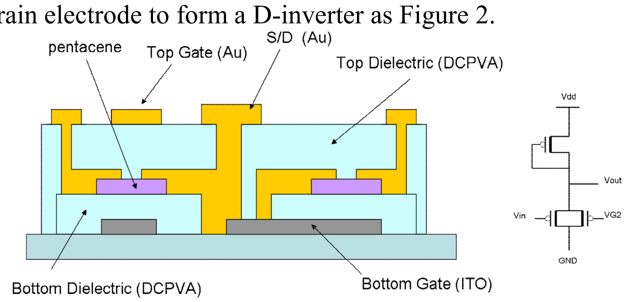

Figure 2 The schematic cross-sectional structures and bias configurations of D-inverter

To analyze the electrical characteristics of PVA and cross-linked DCPVA, we fabricated metal-insulator-metal (MIM) capacitors with a structure of Au (100 nm), gate insulator (600 nm), and ITO (100 nm) on a glass substrate. After the electrical properties of the DG OTFT in the individual device were thoroughly evaluated, the D-inverters were designed based on the transfer characteristics of the individual transistor. The current- voltage (I-V) characteristics were measured with a HP 4156 semiconductor parameter analyzer and the C-V characteristics were determined using a HP 4284 impedance analyzer. All the measurements were performed under dark and shielded conditions.

The dielectric properties of the DCPVA gate dielectric samples with different ammonium dichromate contents measured in the range of 100 Hz to 100 kHz is shown in

Figure. 3. An important concern with gate dielectric materials is the gate leakage current. The results demonstrated that the dielectric constant increases with increasing ammonium dichromate content in PVA, being situated in the range between 5 and 8. Figure 3 shows the leakage current of dielectric film as a function of an ammonium dichromate concentration in PVA solution. It is noteworthy that the presence of the ammonium dichromate concentration causes significant change in the leakage current of dielectric film. This result is associated with the residual of Cr(VI) in the DCPVA film for incompletely reaction of an electron transfer between Cr(VI) and the organic polymeric matrix PVA when the ammonium dichromate content is exceed 4wt%. However, the leakage current of dielectric film increased with the decreasing ammonium dichromate content less than 4 wt%. The reason for this shortcoming is that the cross-linking reaction is not enough to form a homogeneous and rigid film. It is for reason that we choose the optimum concentration 4wt% DCPVA as the dielectric and passivation layer to fabricate our device DG-OTFT.

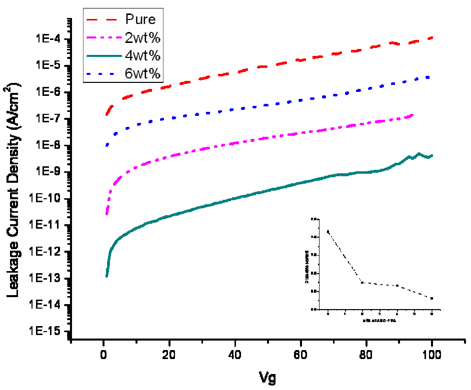

Figure 3 The leakage current of dielectric film with different ammonium dichromate concentrations (an inset that show the dielectric properties of the DCPVA gate dielectric samples with different ammonium dichromate contents)

After top-gate dielectric, DCPVA, was spin-coated on top of the pentacene active layer and then top-gate electrode was deposited on the DCPVA layer, two types of OTFT are available. We designated the DG-OTFT (W/L = 200/50μm) whose drain current-voltage characteristics working at the same operation condition (Vg=-30V) exhibited better current saturation as well as a negligible contact resistance, as presented in Figure. 4. We discovered the DG-OTFT had a V_T as a function of the gate voltage. The on/off current ratio of DG-OTFT is twice as large as conventional OTFT under an optimum gate bias.

Figure 5 shows the voltage transfer current of the D-inverter as schematically presented in Figure. 2. With the supply voltage, *V*dd and *V*in are biased positively, a good inversion of the input signal at the output is observed as shown in the plot of V_{out} vs. $V_{in.}$

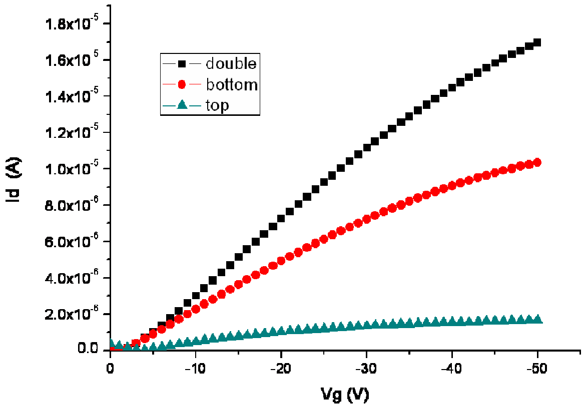

Figure 4 Output characteristic (I_{ds}–V_{ds}) for the bottom gate OTFT (circles), the top gate OTFT (triangles) and DG-OTFT (squares) with channel size *L*=50um, *W*=200 um.

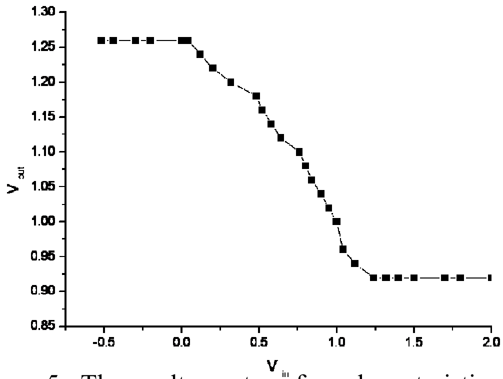

Figure 5 The voltage transfer characteristics of the D-inverter composed of a double-gate driver transistor and a single-gate load transistor as a function of top-gate bias (V_{G2}).

3. Conclusions

Due to the use of top-dielectric and electrode layer on the top of pentacene, the performance of DG-OTFT significantly increased. In summary, we demonstrate the DG-OTFT with low temperature solution process to pattern the D-inverter circuit using photosensitive DCPVA as a bottom-gate dielectric and a top-gate dielectric.

Acknowledgements

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