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Current Reduction Mechanism of Organic Thin Film Transistor

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1. Introduction

Organic Thin Film Transistors (OTFTs) were first demonstrated about 25 years ago [1-3], and today are believed to have remarkable possibilities in realizing flexible devices and printable devices [4-6]. However, the characteristics are generally quite inferior as compared with conventional inorganic semiconductor devices, which are usually attributed to low carrier mobility [7]. Here, numerical simulation was carried out to investigate the actual cause of the inferior characteristics of OTFT's, and to propose improved OTFT structures as well as directions for future technology developments.

2. Numerical Simulation

Device Structure

The device structure used in this study is schematically shown in Fig. 1, where channel length (L), gate oxide thickness (Tox), semiconductor layer thickness (Ts) and impurity concentration (p), heavily doped layer thickness (Tp+) and impurity concentration (p+) were chosen as parameters. Channel width was set constant at 10 μm. The major difference from conventional OTFT structure is the existence of the heavily doped (p+) layer at the contact region, which is inevitable for a silicon TFT because of the contact resistance problem, however, it usually does not exist in OTFT mainly due to available materials limitations.

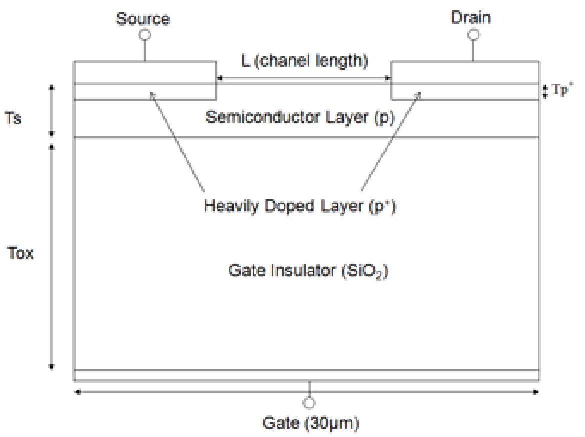

Fig. 1 Schematic cross section of OTFT device used in the simulation

Simulation Method

Device simulation was carried out using the semiconductor device simulation program based on Poisson's equation and continuity equation, which is reported elsewhere [8]. Carrier mobility was set constant at 0.3 cm^2/Vs, and the contact resistance does not exist in this model. Thus, any result derived from this simulation is the intrinsic characteristics of the OTFT's.

3. Results and Discussion

Channel length dependence of OTFT characteristics

Channel length dependence of OTFT characteristics is shown in Fig. 2, for OTFT's with and without p+ layer at a gate voltage (Vg) of 50V, where p is set at 10^{15} cm^{-3}, and p+ at 10^{20} cm^{-3}. These results clearly indicate that the characteristics are superior for devices with p+ layer, and the shorter the channel length, the more the differences in drain current become between devices with p+ layer and those without p+ layer. As indicated previously, contact resistance, barrier between the semiconductor layer and metal contacts and other parasitic effects are not taken into this model, as well as the mobility is kept constant regardless of the device structures. Therefore, this phenomenon reflects intrinsic physical phenomena inside the OTFT.

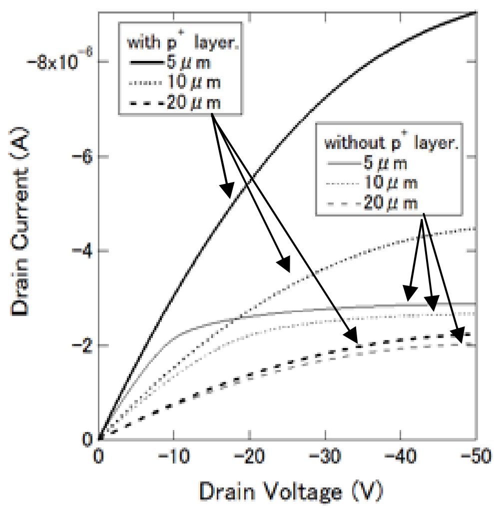

Fig. 2 Channel length dependence of OTFT characteristics for with p+ layer (dark) and without p+ layer (light)

Impurity concentration dependence of OTFT performance

Dependence of OTFT characteristics on the impurity concentration of the semiconductor layer is shown in Fig. 3 at Vg=50V, where the I-V curves are almost the same for OTFT's with p+ layer regardless of impurity concentration, whereas current level decreases to less than 1/100 for those without p+ layer, when the concentration is 10^{12} cm^{-3}. In other words, the apparent mobility becomes less than 1/100 of the actual value if the impurity concentration in around 10^{12} cm^{-3}. This implies that the previously reported experimental mobility values do not necessarily reflect the actual values.

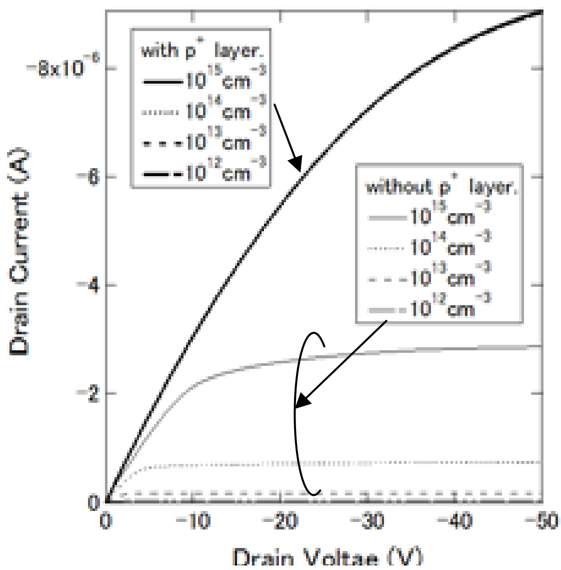

Fig. 3 Dependence of OTFT characteristics on the impurity concentration of the semiconductor layer for with p+ layer (dark) and without p+ layer (light)

Cause of the inferior characteristics without p+ layer

The current reduction mechanism for devices without p+ layer was analyzed, and was attributed to the potential drop at the source-channel interface, which is experimentally ascertained by Ikeda, et al [9]. On the other hand, no potential drop was observed for devices with p+ layer. The origin of this potential drop was attributed to carrier deficiency at the channel region, as indicated in Fig. 4(a), as compared with the results for devices with p+ layer shown in Fig. 4(b). The carriers are usually supplied from the p+ layer in Si TFT's, whereas no carrier source exists in conventional OTFT's. Therefore, the cause of the inferior characteristics of OTFT is the lack of p+ layer, which supplies carriers to the channel region.

3. Conclusions

The current reduction mechanism of OTFT was analyzed using device simulation, and was attributed to the deficiency of carriers in the channel region, which are otherwise supplied from the heavily doped layer under the contact region. The present OTFT's do not have such p+ layer, because of the restrictions of materials. Therefore, these results clearly direct the directions of technological developments for improving OTFT characteristics.

Acknowledgements

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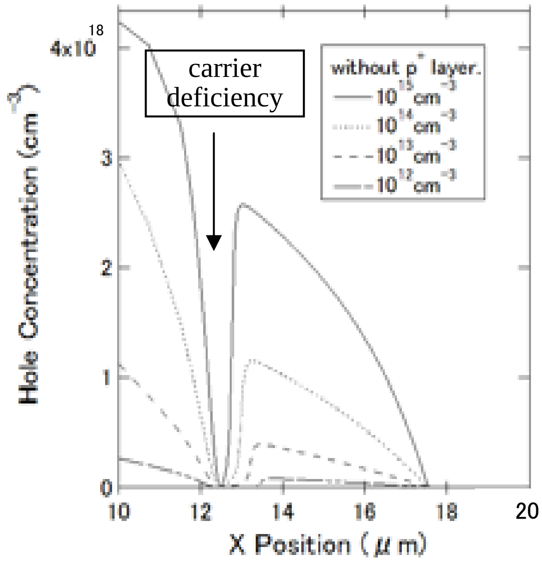

Fig. 4(a) Carrier concentration around the source-channel interface for devices without p+ layer

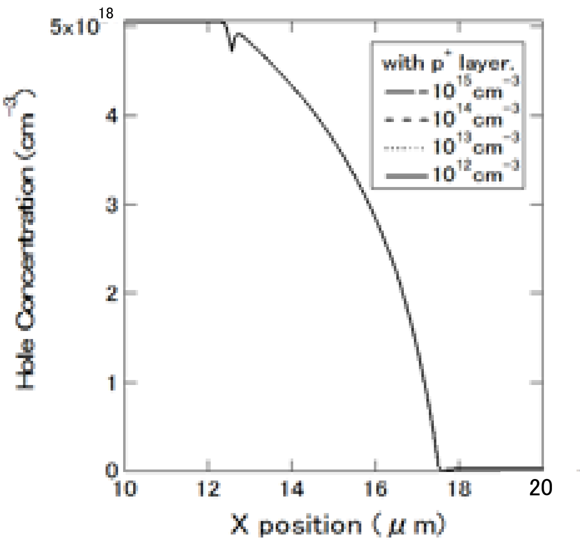

Fig. 4(b) Carrier concentration around the source-channel interface for devices with p+ layer

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