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Overview and Future Challenges of Capacitor-less DRAM Technologies for High Density Memory Applications

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1. Introduction

Scaling 1T/1C DRAM bit cells below the 50 nm node dimension represents a serious challenge. Contacts, devices aspect ratios and capacitor materials approach manufacturing limits. Recently, new concepts have been proposed to address these scaling and performance limitations. Among them, the capacitor less RAM cell is one of the leading contenders as it is simple, uses only conventional materials and is therefore fully compatible with CMOS processes. Following the introduction of a technology exploiting a BJT operation, capacitor-less RAM cells are now well suited to replace standalone DRAM cells in sub 50 nm memories.

2. History

Capacitor-less RAM technologies have experienced a drastic evolution over the years. A first version integrating a PMOS transistor on SOS was described by Sasaki et al. [1]. By exploiting the Floating Body (FB) effect of a single NMOS SOI transistor, a simpler and denser structure was proposed by Tack et al. [2]. The device operations described in [1-2] were, however incompatible with selective read/write operations and memory array implementation. Recently, by pulsing the device gate and drain, Okhonin et al. [3-5] and Ohsawa et al. [6] developed the FB Memory (FBM) technology necessary to do the selective write/read operations required in a RAM array arrangement. More recently, as illustrated in Fig.1, by exploiting a BJT operation, Okhonin et al. [7] demonstrated a technology exhibiting a higher signal to noise ratio, a longer retention time, a better scaling ability and full compatibility with future fully depleted 3 Dimensional (3D) devices. This technology has been named Z-RAM® by Innovative Silicon. Due to its improved scalability, the Z-RAM operating principle allows capacitor-less RAM cells to replace standalone DRAMs [7-9].

3. Z-RAM for embedded memory applications

The Z-RAM bit cell and operating principle can be used to build embedded memories [10]. Fig.2 shows the various bit cell layout possibilities for planar structures. Embedded memories allow the integration of cells having a 25 to 45 F^2 area (F being the minimum feature size of the technology).

Fig.3 illustrates a 4 Mbit embedded Z-RAM SRAM cache replacement macro developed for a 45 nm logic process. Read and write latencies of 2 and 4 ns respectively have been demonstrated. Typical device retention times of 100 ms have been achieved (Fig. 4).

4. Z-RAM as standalone DRAM replacement

The Z-RAM bit cell and operating principle can also be used for standalone memory applications [11]. Cell sizes of 4 to 8F2 are possible (Fig.2). Fig. 5 illustrates the case of a 6F2 cell implemented in a 50 nm technology [11]. Such cells integrated with a low leakage process exhibit typical retention times of a few seconds as shown in Fig. 6.

5. Scaling, roadmap & challenges

At 50 nm and below, excessive device leakage resulting from aggressive device scaling severely affects both standby power and retention for DRAM and SRAM technologies. This has prompted 3D structures to enter the memory technology roadmaps. These 3D structures also provide a benefit to floating body memory cells and enables source and drain doping profile engineering to control and improve the cell electrical performance. Due to its unique compatibility with fully depleted devices, the Z-RAM technology is fully portable to all forms of 3D devices such as FinFETs, MuGFETs, surrounding gate transistors (SGT), Tri gate, vertical double gate or gate all around structures. Fig. 7 shows as an example, the programming window and retention time of an 11 nm FinFET device [12].

6. Conclusions

For technology nodes below 50 nm, the standard 1T/1C DRAM bit cells present huge scaling and manufacturing challenges. Due to the simplicity and performance of the floating body memory and the compatibility of the Z-RAM concept with future 3D structures, the Z-RAM bit cell appears as the ideal candidate to replace the standard 1T/1C DRAM bit cell for future high density memory applications.

References

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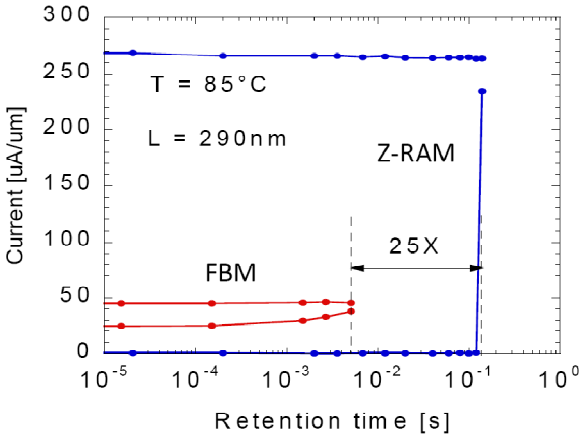

Fig.1: BJT Z-RAM vs regular FBM read current and retention time

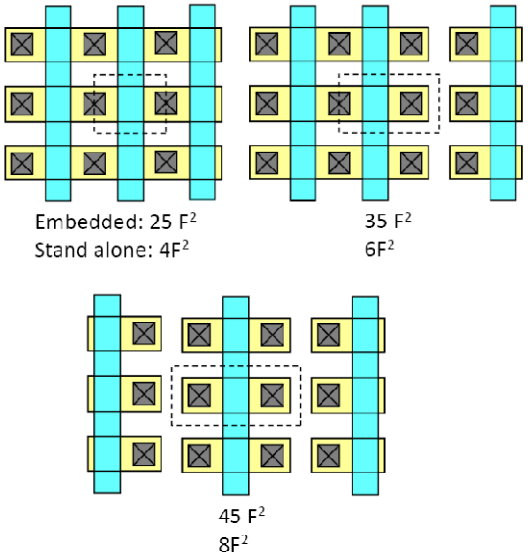

Fig.2: Z-RAM various bit cell layout

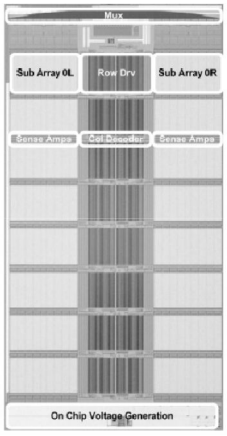

Fig. 3: Picture of a 4Mbit embedded Z-RAM macro

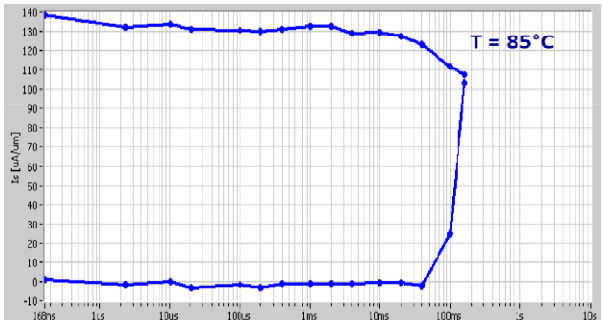

Fig. 4: Typical embedded Z-RAM device retention time

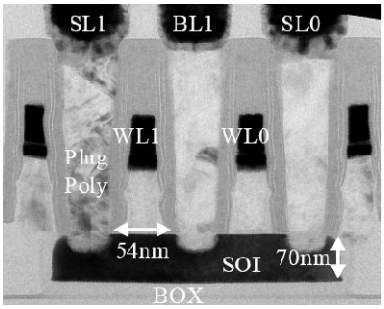

Fig.5: 6F² standalone Z-RAM bit cell cross section

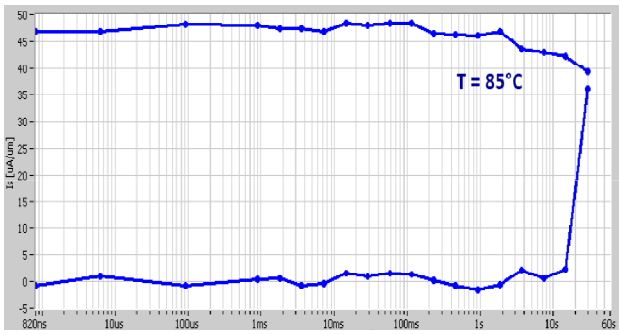

Fig.6: Typical standalone Z-RAM device retention time

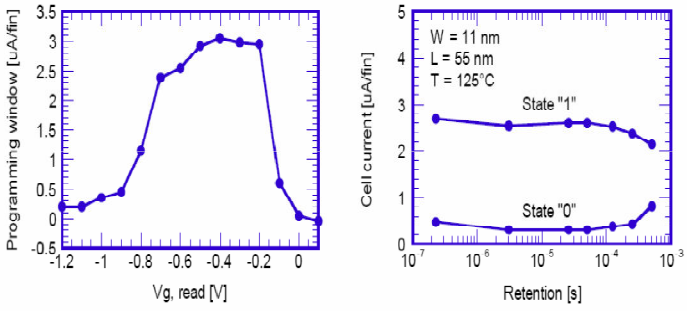

Fig.7: Programming window (left) and retention time (right) for an 11 nm FinFET Z-RAM