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A Highly Scalable $4F^2$ DRAM Cell Utilizing a Doubly Gated Vertical Channel

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Abstract

A double-gate transistor structure with a vertical channel is proposed and demonstrated via 3-dimensional device simulations to be well-suited for DRAM application. The DGVC cell occupies $4F^2$ area, provides for good retention characteristics (with immunity to disturbances), and is compatible with conventional memory process flows for stand-alone DRAM memories. In comparison with previous cell designs, the DGVC cell is more scalable, so that it is an excellent candidate for the continued scaling of DRAM technology to the 22nm node and beyond.

Introduction

The concept of a capacitor-less DRAM cell was proposed to overcome scaling challenges for conventional 1-transistor/1-capacitor DRAM cells [1]. The silicon-on-insulator (SOI) floating body cell (FBC) design [2] offers a small cell size ($4F^2$) but requires more expensive SOI substrates and is difficult to scale to very short channel lengths. The double-gate DRAM (DG-DRAM) cell was proposed as a more scalable design [3] and was recently demonstrated at 70nm gate length [4]; however, it has a relatively large cell size ($8F^2$), is susceptible to disturbance within a memory array, and is not easily integrated into a conventional memory process flow. In order to overcome the deficiencies of previous capacitor-less DRAM cell designs, we propose a new $4F^2$ double-gate vertical channel (DGVC) design that can be fabricated on a bulk-Si wafer using a conventional process flow. The operation and scalability of the DGVC cell are demonstrated via Sentaurus [5] device simulations. Read and write disturbances can be avoided by using appropriate biasing conditions for operation within a cell array.

Device Architecture and Proposed Fabrication Flow

Fig. 1 depicts the DGVC cell and array structure. All of the cells within the array share a common source junction, located at the bottom of the vertical channels. The drain junctions are formed at the top of the vertical channels and are contacted by bit lines, one for each row of cells within the array. Gate lines run orthogonally to the bit lines, and each serves to gate the channels located on either side of it; thus each cell shares its front gate with a neighboring cell along the same bit line, and each cell shares its back gate with the opposite neighboring cell along the same bit line. The circuit schematic of a DGVC cell array is shown in Fig. 2. This array configuration achieves the most efficient cell layout area of $4F^2$. The fabrication process for the DGVC cell array is illustrated in Fig. 3. Key steps are 1) shallow trench isolation (STI) to make stripes of Si along the bit line direction, 2) trench etch to form self-aligned vertical channel structures along the word line direction and 3) etch-back of the deposited metal gate material to form separate front- and back-gate lines [6].

Cell Operation

3-dimensional device simulations were performed to investigate the operation of a DGVC cell with physical design parameters corresponding to 22nm technology as listed in Table I. The cell bias conditions are listed in Table II, for Write, Hold, and Read operations. During a Write "1" operation, holes are generated by impact ionization and accumulate in the body region at the back channel interface; during a Write "0" operation, any holes in the body region are removed through the drain. During a Hold operation, the cell is biased to form a potential well to retain holes in the body region.

The state of the cell is determined by sensing the drain current during a Read operation: if holes are stored in the body, the threshold voltage will be lowered and hence the drain current will be higher. This can be seen from Fig. 4, wherein the current levels for the "1" state and the "0" state can be clearly distinguished (by a margin of at least 2μA) for a storage time as long as 200ms at 85°C. These results indicate that the DGVC cell can meet retention requirements for stand-alone memory applications. Fig. 5 shows that a DGVC cell can be read non-destructively multiple times, so that a refresh operation is not necessary after each read cycle.

In previous works [4], a negative bit-line voltage was used to apply forward-bias on the body-drain diode to sweep out the accumulated holes during a Write "0" operation. This inevitably disturbs unselected cells in the "1" state that are connected to the same bit line. We propose instead to use a self-converging purge mechanism to avoid significant disturbance issues [3]: when the drain bias and back-gate bias are set to zero (V_d=0V and V_{bg}=0V) while applying a small positive source bias (V_s=0.5V), the potential barrier between the body and drain at the back channel interface is reduced so that excess holes in the body region flow out to the drain; this causes the potential barrier to increase and hence the flow of holes to decrease, so that a steady-state condition (zero hole flow) is eventually reached. This biasing scheme allows a sufficient current margin to be maintained for unselected cells that share the same back-gate line (ref. "C" in Fig. 3), for a write time as long as 5μs (Fig. 6a). Disturbance of unselected cells along the same bit line (ref. "A" and "B" in Fig. 3) can be avoided by applying negative gate biases (ref. Table II) to maintain the hole potential barriers within these cells.

A Write "1" operation can potentially disturb unselected cells in the "0" state that are connected to the same bit line (ref. "A" and "B" in Fig. 3). This issue can be avoided by appropriately biasing the gate lines (ref. Table II) to maintain the unselected cells in the off state (Fig. 6b).

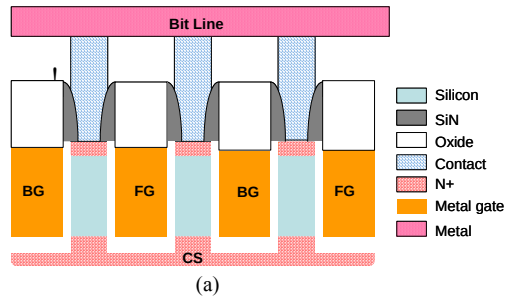
Scalability

In order to investigate the scalability of the DGVC cell, read currents were simulated for cells with body thickness scaled proportionately with the technology node. Fig. 7a shows how the read currents depend on the channel length, for each state. Fig. 7b shows that the optimal channel length for maximum current sensing margin scales with the body thickness, and that the optimal channel length is 80nm for a 22nm technology. At longer channel lengths, the "1" state current is lower, and at shorter channel lengths, the "0" state current is higher due to the effect of drain-induced barrier lowering (DIBL). A reduced body thickness reduces the DIBL effects and allows for a shorter channel length to increase the sensing margin.

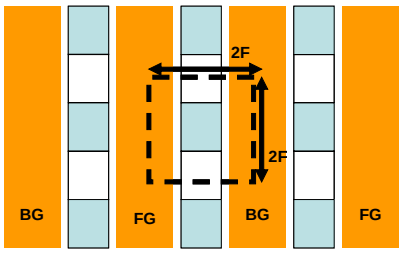
Fig. 8 compares the dimensions of the DGVC cell design vs. the planar DG-DRAM cell design, for the same technology nodes. It has been reported previously that channel length scaling of the planar DG-DRAM cell is limited to ~25nm due to significant quantum confinement effects for body thicknesses below 4nm [7]. Because the DGVC cell allows for longer channel lengths at a given technology node, it is a much more scalable design.

Conclusion

A doubly gated vertical channel transistor structure is proposed as a highly scalable $4F^2$ DRAM cell design, one which can be fabricated using a conventional process flow sequence. Retention and disturbance immunity characteristics of a DGVC cell are shown to be adequate for stand-alone memory applications, at the 22nm technology node (0.00194 μm^2 cell size). The vertical channel design allows for longer channel lengths as compared to a planar channel design, so that it is promising for $4F^2$ DRAM scaling to sub-22nm technology nodes.



(a)



(b)

Fig. 1 (a) Schematic cross-sectional view of DGVC cells (parallel to the bit line) (b) Schematic plan view of DGVC array

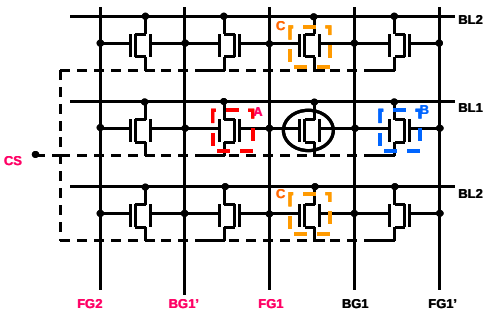


Fig. 2 Circuit schematic of a DGVC cell array

	Write "1"	Write "0"	Hold	Read
FG1	1.5V	0.0V	-1.0V	1.5V
BG1	-1.0V	0.0V	-1.0V	-1.0V
BL1	2.0V	0.0V	0.5V	0.7V
CS	0.5V	0.5V	0.5V	0.5V
BL2	0.5V	0.5V	0.5V	0.5V
FG1'	-1.0V	-2.0V	-1.0V	-2.0V
BG1'	-2.5V	-2.0V	-1.0V	-2.5V
FG2	-1.0V	-1.0V	-1.0V	-1.0V
Time	20ns	20ns	100ms	20ns

Table II. Bias conditions

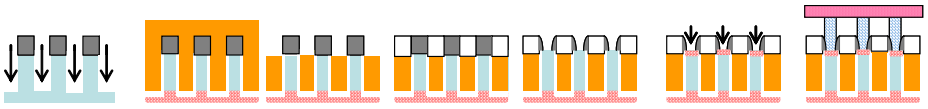


Fig. 3 Key process steps for DGVC array: 1) STI formation along the bit line direction, 2) Trench formation and buried source implantation (not shown), 3) Gate material deposition, 4) Gate etch-back, 5) Capping oxide deposition and CMP, 6) Nitride removal, spacer formation, 7) drain implantation, and 8) Contact formation.

Parameters	
Technology node = 22nm	Cell Size = 0.000484 um² (4F²)
N_{body} = 10^{16} cm^{-3} (p-type)	$N_{S/D}$ = 10^{20} cm^{-3} (n-type)
T_{ox} = 40 Å	T_{body} = 200 Å
$L_{channel}$ = 50nm (Si-pillar height)	W_{active} = 22nm (Si-pillar width)
$\tau_{electron}$=1.5 µsec	τ_{hole}=1.5 µsec

Table I. Simulated cell parameters

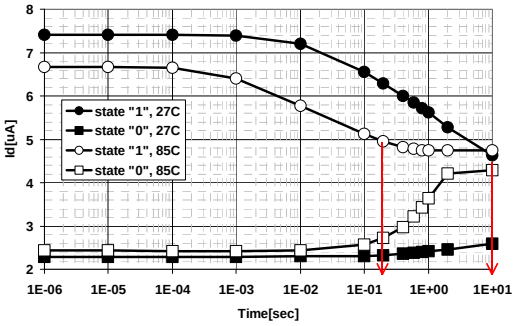


Fig. 4 Retention characteristics of a DGVC cell (The read and write times are 20nsec)

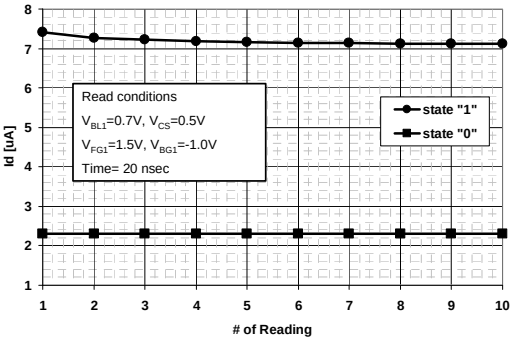
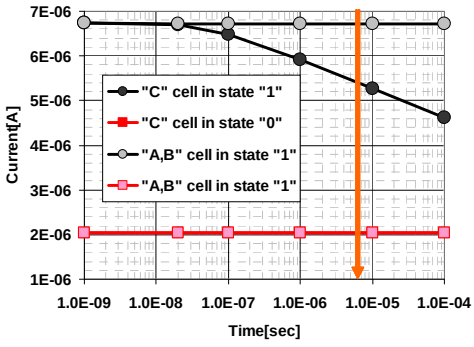
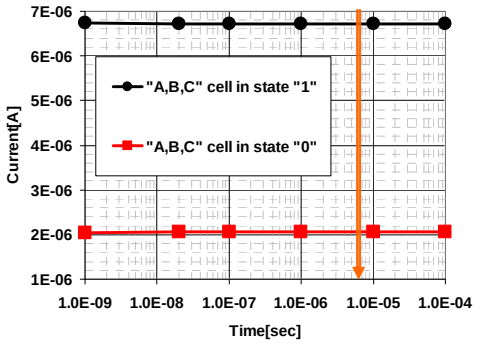


Fig. 5 Non-destructive readout characteristic of a DGVC cell

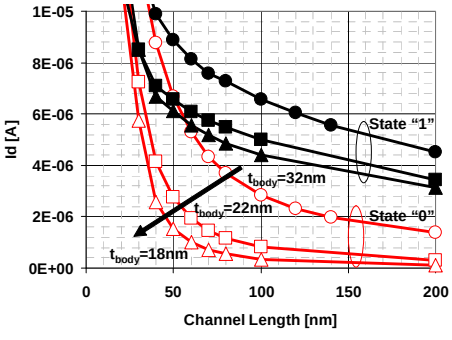


(a)

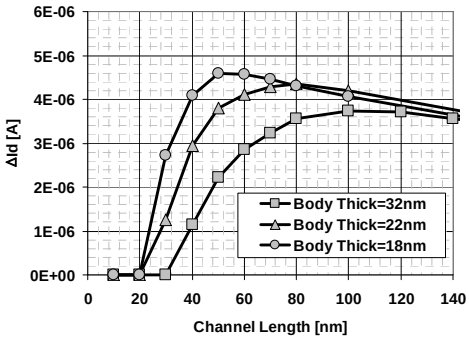


(b)

Fig. 6 (a) Write "0" disturbance on the unselected cells (b) Write "1" disturbance on the unselected cells. The indicated total disturbance time (5 µsec) is derived by assuming 20nsec read time and 128(WL) x 256(BL) array



(a)



(b)

Fig. 7 (a) Readout currents for State "1" and State "0" (b) Current differences between "1" and "0" states. Thinner body thickness suppresses the DIBL effect and provides for shorter optimal channel length which increases the sensing margin. The read and write times are 20 nsec.

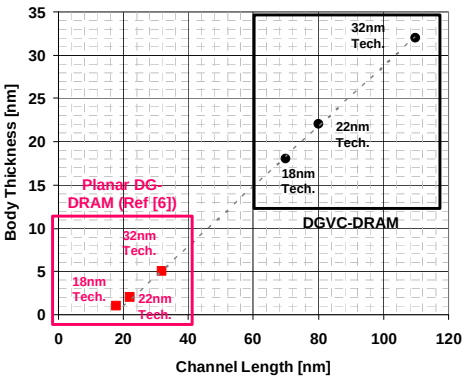


Fig. 8 Required body thickness for a given channel length. As compared against planar DG-DRAM cells, DGVC DRAM cells can have longer channel lengths and greater body thickness at a given technology node.

References

[1] H. Wann and C. Hu, "A Capacitorless DRAM Cell on SOI Substrate", pp 635-638, IEDM 1993.
[2] S. Okhonin et all, "A SOI capacitor-less 1T-DRAM concept," in Proc. IEEE Int. SOI Conf., pp. 153–154, 2001.
[3] C. Kuo, T. King and C. Hu, "A Capacitorless double gate DRAM technology for sub-100-nm embedded and stand-alone memory applications," in IEEE TED, Vol. 50, 2003.
[4] I. Ban et al, "Floating Body Cell with Independently-Controlled Double Gates for High Density Memory", Symposium on VLSI, 2007.
[5] Sentaurus Ver. A-2008.09, SYNOPSYS
[6] T. Schloesser et all, " 6F2 buried wordline DRAM cell for 40nm and beyond", IEDM, 2008.
[7] N. Z. Butt et all, "Scaling Limits of Double-Gate and Surround-Gate Z-RAM Cells" IEEE TED, Vol. 54, 2003.