Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp144-145

Highly Scalable Capacitorless DRAM Cell on Thin-Body with Band-gap Engineered Source and Drain

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1. Introduction

As DRAM technology shrinks down to sub 50nm node[1], fabricating conventional 1T/1C DRAM cell faces significant challenges due to high process complexity when integrating a large capacitor. Recently, 1T DRAM utilizing floating body as a charge storage element, which is compatible with CMOS technology, has been proposed and attracted much attention[2-3]. However, with the cell size scaling down, the sensing current and retention time are decreased[4], due to the physical limit of body potential variation(ΔV_{BS}) and drain induced barrier lowering (DIBL) effect. Thus, wide devices or multi fins are needed to obtain the required signal margin, which will decrease the memory density.

In this paper, a novel band-gap engineered source and drain floating body cell (BE-FBC) for high density embedded DRAM applications is proposed and investigated for the first time. Compared with the conventional FBC, the BE-FBC can break the physical limit of ΔV_{BS}, thus greatly improving the electrical performance. It is observed that BE-FBC can yield 3-4 times larger signal margin and better retention behavior. In addition, the scaling capability is also studied. The results show that BE-FBC exhibits more significant improvement for shorter channel length (L_G), showing great potentials for further scaled generations.

2. BE-FBC concept and operation

The BE-FBC targets the enhancement of source/drain(S/D) -body barrier for higher body potential variation. The floating body is formed by intrinsic potential well with the lateral N-P-N junction in the FBC. Charges stored in the well can change the body potential V_{BS}, thus resulting current variation. However, the ΔV_{BS} is physically restricted due to the limited potential well height formed by silicon(Si) P-N junction between the S/D and floating body. To break this physical limit, BE-FBC utilizes wide band-gap material Si_xC_{1-x} as the source/drain. Silicon-Carbon (Si_xC_{1-x}) S/D have been evaluated as the efficient stressor to enhance the drain current in SOI MOSFET devices [5-6]. In this work, we investigate Si_xC_{1-x} S/D for improving the electrical performance in the FBC. The cross-sectional view of the proposed BE-FBC is shown in Fig.1. The deeper potential well(shown in Fig.2) formed with the Si_xC_{1-x}-Si hetero junction can effectively reduce the hole leakage when the cell is programming and holding, and thus better performance can be obtained. Fully depleted Silicon-On-Insulator (FDSOI) architecture with light-doped ($1\times10^{16}cm^{-3}$) thin body (30 nm) and thin BOX(10nm) is studied by numerical simulation using device simulator Sentaurus. Midgap metal gate and P-type polysilicon back gate are adopted. Writing “1” is performed by impact ionization with positively biased gate(V_G) and drain(V_D), and state “0” is obtained by forward biased drain-body junction. The operation wave form of applied bias is shown in Fig.3.

3. Results and Discussions

Fig.4 shows the output characteristics of the conventional FBC and BE-FBC. The kink effect of the BE-FBC is much more prominent than the FBC, showing greater potentials to improve the cell performance. Fig.5 shows the simulated hole density at state “1” in the FBC and BE-FBC. It can be seen that more charges are stored in the BE-FBC, which can enhance the sensing current as shown later. Physical mechanism of the more stored charges is studied. When writing “1”, holes generated by impact ionization can raise the body potential, and then some holes will flow out of the body through forward biased S/D-body junction. This hole leakage current will reduce hole density stored in the body, thus decreasing sensing current. In Fig.5 it can be observed the hole current at the source in the BE-FBC is 2 or 3 orders lower than the FBC when applying a programming pulse. The smaller leakage current can increase hole density in the body, when reaching dynamic equilibrium.

Fig.6 illustrates the drain current with write/read operations. It can be observed that with similar “0” state reading current, “1” state reading current of the BE-FBC is much higher. The current difference of BE-FBC is about 3 times larger than the FBC. As shown in Fig. 8, the retention characteristics of BE-FBC is also very good. The sensing current of BE-FBC at 100ms after writing “1” is about 27μA/μm, which is close to the initial sensing current of the FBC. The operating transient drain current and retention characteristics of 0.05μm BE-FBC are shown in Fig.9 and Fig.10. Large sensing current and good retention behavior are also obtained due to this novel band-gap engineered potential well. With similar structure as the conventional FBC, $6F^2$ BE-FBC can be easily realized as shown in Fig.11. BE-FBC with large signal current and good retention characteristics is suitable for high density DRAM applications. The conventional FBC is difficult to achieve high density, since wide devices are needed to ensure the required sensing margin. Fig.12 shows comparisons of programming window with different gate length. The sensing margin of the conventional FBC is degraded drastically as the cell scales down due to the physical limit and severe DIBL effect. However, large sensing current is still observed of BE-FBC with 0.03um gate length, which demonstrates BE-FBC have much better scalability than the conventional FBC.

4. Conclusions

For the first time, a novel capacitorless DRAM cell with band-gap engineered S/D is proposed and investigated. The band-engineered S/D is compatible with strain CMOS technology. Compared with the conventional FBC, the BE-FBC can achieve much larger sensing current and better retention behavior, which is suitable for high density DRAM applications. In addition, the channel length dependence of sensing current illustrates that BE-FBC has larger programming window in very short channel device, showing great potentials for high density DRAM applications in highly-scaled era.

Acknowledgements

This project is supported by National Natural Science Foundation of China (60625403 and 90707006), and by 973 Projects of China (2006CB302701).

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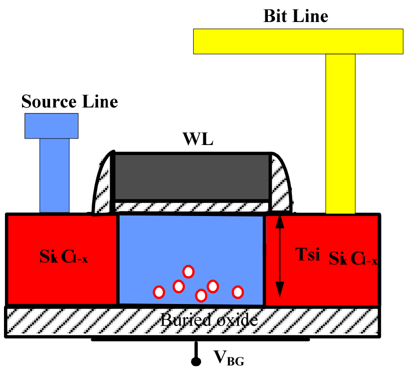


Fig.1 The proposed novel BE-FBC with Si_xC_{1-x} band-gap engineered source/drain.

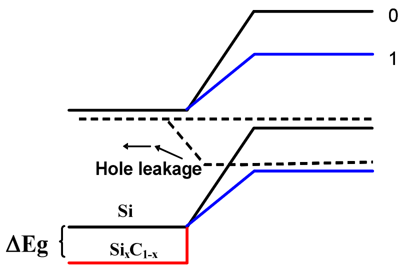


Fig.2 Energy band of the conventional FBC and BE-FBC at state "0" and "1", hole leakage current at state "1"

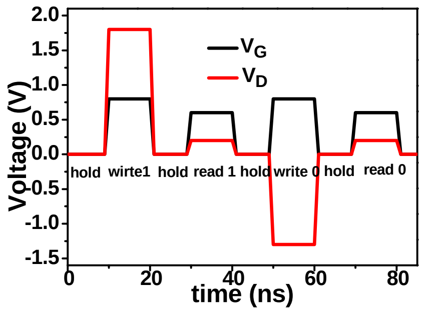


Fig.3 Waveform of the applied biases during reading and writing. The Back gate V_{BG} and the source V_S is kept at -1 V and 0 V, respectively.

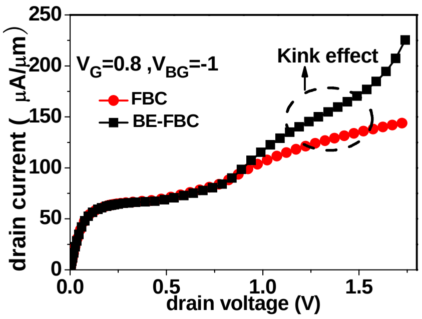
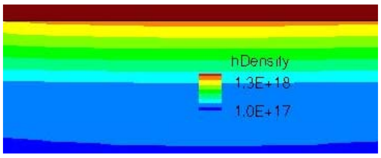
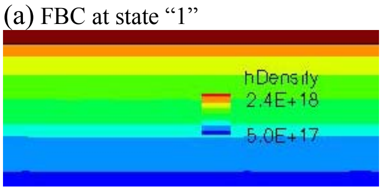


Fig. 4 Output curves of the cells. Kink effect of BE-EBC is clearly seen and more apparent than the conventional FBC



(a) FBC at state "1"



(b) BE-FBC at state "1"

Fig.5 Hole density in the floating body at state "1". Higher hole density is found in the BE-FBC

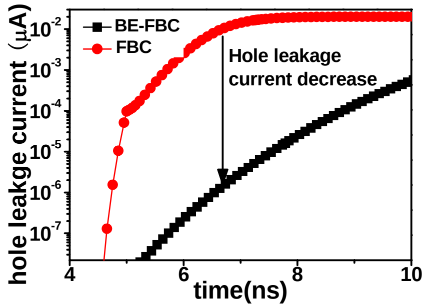


Fig.6 Hole leakage current at the source while applying a writing "1" pulse.

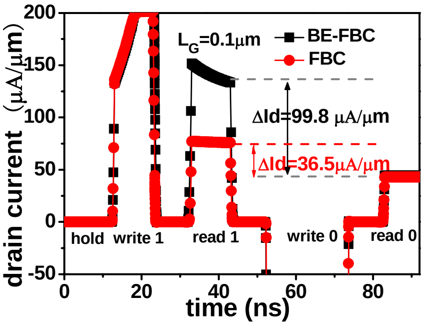


Fig.7 Read and write currents of 0.1 um cells. The sensing current of the BE-FBC is 3 times larger than the FBC.

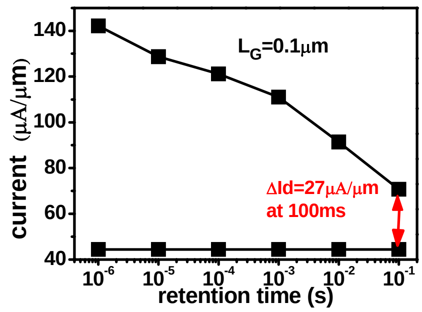


Fig.8 Data retention characteristics of the BE-FBC with L_G=0.1μm (hold condition: V_D=V_S=0V, V_G=-0.5V, V_{BG}=-1 V)

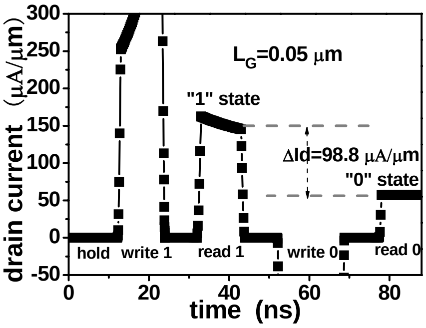


Fig.9 Drain current time dependence during read, write for the BE-FBC with L_G=0.05μm

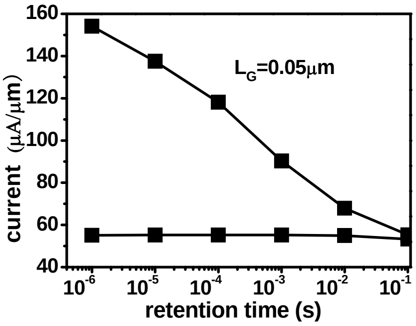


Fig.10 Retention characteristics of the BE-FBC with L_G=0.05μm (hold condition V_D=V_S=0V, V_G=-0.5V, V_{BG}=-1 V)

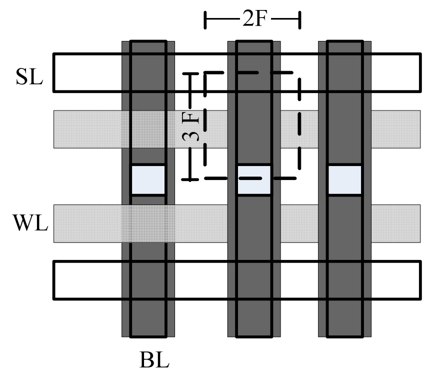


Fig.11 Layout of BE-FBCs, $6F^2$/cell can be obtained.

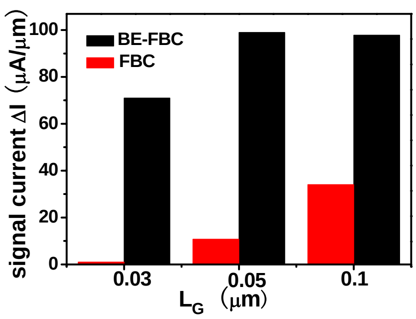


Fig.12 Comparison of the sensing current with different gate length between the FBC and BE-FBC