Performance Improvement of the Capacitorless DRAM Cell with Quasi-SOI Structure Based on Bulk Substrate

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1. Introduction

With the aggressive increase of the demands for high density and high performance DRAM, the traditional one-transistor and one-capacitor (1T/1C) cell faces many problems, such as the requirement for high K dielectric and high aspect ratio etching process. Recently, capacitorless DRAM cell has been proposed and attracted much attention due to its simple 1T structure and good compatibility with CMOS process [1, 2]. In order to form the floating body region, most capacitorless cells are based on SOI substrate, which limits its application and development. To circumvent this, 1T-bulk cell has been proposed [3, 4]. However, the improvement for sensing current and retention performance is still needed for 1T-bulk cell. In addition, the cell requires larger area, compared with the cell based on SOI substrate.

In our previous works, quasi-SOI (QSOI) structure was proposed [5, 6]. It can be fabricated on bulk substrate and suitable for logic and analog/RF applications in highly scaled era. Based on this promising structure, a novel QSOI capacitorless DRAM cell is proposed and investigated for the first time. Compared with bulk cell, QSOI cell can achieve better electrical performance and smaller cell area, showing great potentials for high density DRAM applications.

2. Cell structure and operation

The cross-sectional view of the proposed QSOI capacitorless DRAM cell is shown in Fig.1. The new 1T DRAM cell is based on QSOI structure with source/drain surrounded by an L-shape localized insulator. Similar to 1T-bulk cell, a deep N well (DNW) is used to isolate the floating body region to substrate. QSOI device can be fabricated on bulk substrate with a process which is basically compatible with CMOS technology. Fig.2 gives the process flow and the SEM image of the fabricated device. By adding an N-layer implantation step, the QSOI DRAM cell can be easily realized based on the fabrication process of the QSOI device. Simulation has been performed with device simulator-Sentaurus. The 0.18µm device is studied with 5nm gate oxide. The impact ionization mechanism is used for writing "1" with positively biased gate and drain. For comparison, the bulk cell is also studied. The two different cells have the same structure parameters except the L localized insulator around the S/D region in QSOI cell.

3. Results and discussion

Fig. 3 shows the electrostatic potential distribution in the QSOI cell. It can be obviously seen that the potential of the floating body is raised at state "1" due to the stored holes generated by impact ionization. This also verifies the feasibility of the simulation method. In Fig. 4, the operation conditions during reading and writing are given. The corresponding transient drain current is also shown. The cells can be written to "1" state in 10ns. After that, the drain current saturates, showing that a dynamic equilibrium is reached. With the similar "0" state reading current, the QSOI cell can achieve larger "1" state reading current, and thus larger sensing current. During writing, the impact ionization generated holes flow to the body to raise the body potential just like a current source as shown in Fig. 5 [4]. As the body potential rises, the leakages through the pn diodes increase, as shown in Fig. 5. The dynamic equilibrium is reached when the body node current is zero. In QSOI cell, the L-shape isolation can decrease the area of the leakage path between body and source/drain. Therefore, more holes can be stored in the body region of the QSOI cell at dynamic equilibrium. More stored holes in QSOI cell result in larger $V_{\rm th}$ shift due to the body effect, and thus larger sensing current as shown in Fig. 6.

Non-destructive reading is one of the advantages of the capacitorless DRAM. The retention characteristics are investigated under continuous reading condition as shown in Fig. 7. The QSOI cell with 30nm L thickness can achieve larger I_d difference which can relaxes the requirement for sensing circuits. As shown in Fig. 8, the retention characteristics can be significantly improved by thinning the L-shape isolation, which can increase the refresh interval. Compared with bulk cell, about five times longer retention time can be obtained in the cell with an L-shape isolation thickness of 10nm with 6μ A detection threshold. The cell with a thin L-shape isolation can be easily fabricated by optimizing the time of the L-shape oxidation.

For high density DRAM applications, cell area is one of the main concerns. In bulk cell, STI is used for lateral isolation which increases the cell area. In order to decrease the cell area, the deep L-shape isolation structure is proposed as shown in Fig. 9. In this structure, the L-shape layer can provide isolation between adjacent cells along bit line. Moreover, the deep L-shape structure makes it feasible to share source/drain for the adjacent cells, which can further decrease the cell area. The cell area comparison between bulk and QSOI cells is shown in Fig. 10. Utilizing QSOI structure, $6F^2$ cell can be designed with 40% saved area compared with the bulk cell. The retention characteristics can be maintained in the cell with deep L-shape isolation as shown in Fig. 11.

4. Conclusions

In this work, a novel QSOI capacitorless DRAM cell with bulk substrate is proposed and investigated. QSOI structure is one of the candidates for logic and analog/RF applications in highly-scaled era. Based on the promising structure, the proposed cell can achieved better retention characteristics and larger sensing margin. In addition, 40% cell area can be saved compared with bulk cell. The results show that QSOI cell has great potentials for high density DRAM applications.

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Fig. 1 Capacitorless DRAM cell with QSOI structure with raised deep n well based on bulk substrate. The S/D is surrounded by L shape localized insulator.



Fig. 4 Waveform of the applied biases during reading and writing and the corresponding transient drain current of the QSOI cell and bulk cell.



Fig. 7 Retention characteristics of the cells with different structures under continuous reading condition.





Fig. 2 Fabrication process flow for QSOI structure and the cross sectional SEM image. Capacitorless DRAM cell can be easily fabricated by additional n-layer implantation.



Fig. 5 Equivalent circuit of the capacitorless DRAM cell based on bulk substrate during writing 1. The impact ionization mechanism can be considered as a current source.



Fig. 8 Retention time of the QSOI cells with different L layer thicknesses under continuous reading condition. The detection threshold is 6μ A.



(a) (b) Fig. 3 Electrostatic potential distribution in the QSOI cell at state "0" (a) and state "1" (b). The body potential is raised at state "1" due to the stored holes.



Fig. 6 Transfer curves of the cells with different structures. QSOI cell can achieve larger Vth shift and thus larger read current difference.



Fig. 9 Cross sectional view of the modified QSOI cell with deep L-shape isolation. Deep L-shape oxide layers are used as floating body isolation for adjacent cells along bit line.



Fig. 10 Layouts for the QSOI cell with deep L-shape structure (a) and the bulk cell (b). The L-shape layer can provide common source/drain design and remove STI for the adjacent cells, resulting in cell area shrinking.

Fig. 11 Retention characteristics of the QSOI cell with deep L-shape isolation.