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Seed layer and multistack approaches to reduce leakage in $SrTiO_3$-based MIM capacitors using TiN bottom electrode

N. Menou[1], M. Popovici[1], K. Opsomer[1,2], B. Kaczer[1], M. A. Pawlak[1], A. Franquet[1], C. Detavernier[2], S. Van Elshocht[1], D. J. Wouters[1], S. Biesemans[1] and J. A. Kittl[1]
[1] IMEC, kapeldreef 75, B-3001 Leuven, Belgium
Phone: +32-16-28-10-69; E-mail: nicolas.menou@imec.be
[2]Ghent University, Krijgslaan 281/S1, B-9000 Ghent, Belgium

1. Introduction

Leakage reduction is crucial for MIM capacitors for future DRAM nodes. In previous investigations we showed that increasing the Sr-content would result in leakage reduction of $SrTiO_3$ (STO) films deposited on TiN [1]. In this work we demonstrate for thin (10nm) stoichiometric $SrTiO_3$ films that the leakage properties can be significantly lowered (while keeping high capacitance densities) by using stacking approaches such as seed layer (thin STO layer crystallized before the "bulk" STO deposition) and multistack STO/$GdAlO_3$/STO (Fig. 1).

2. Sample fabrication and physical analysis

$SrTiO_3$ layers were deposited by atomic layer deposition (ALD) in a cross-flow ASM Pulsar® 3000 reactor, at reactor temperatures of 250°C [2]. The precursors were $Sr(t\text{-}Bu_3Cp)_2$, H_2O, and $Ti(OCH_3)_4$ [2,3]. Stoichiometric STO films in the 10-20nm range were grown on TiN with good thickness and composition control over 300mm wafers [2]. Careful characterization of the $SrTiO_3$ crystallization behavior was achieved for the different stacks by in-situ XRD during ramp anneals in He (Fig. 2). At low temperature, $SrTiO_3$ peaks are observed only when a seed layer approach was used. This indicates that the seed was crystalline after anneal at 700°C in N_2 as confirmed in Fig.3a. The use of that crystalline seed helps to drastically lower the crystallization temperature of the "bulk" $SrTiO_3$ to ~420°C (T_{cryst}~520°C for STO directly deposited on TiN) as shown on Fig.2 and Fig.3b. On the other hand, insertion of 1nm $GdAlO_3$ (deposited by ALD at 250°C) between two 7nm $SrTiO_3$ layers slightly increases the crystallization temperature of $SrTiO_3$. At high temperature, all films/stacks crystallized into the high-k perovskite $SrTiO_3$ phase. Those results imply two consequences regarding the crystallization anneal of the layers: (1) the low T_{cryst} obtained for the seed layer approach makes it possible to use crystallization anneals in O_2 even with TiN bottom electrodes. (2) Only N_2 anneals can be considered for crystallization of STO/$GdAlO_3$/STO stacks to avoid any damage (oxidation, roughening…) of the TiN bottom electrode. Nevertheless, considering the relatively high temperature (~600°C) required for crystallization of STO/$GdAlO_3$/STO stacks, one has to make sure that no major intermixing occurs between the constituting elements of the stack. Fig.4 shows time-of-flight secondary ion mass spectroscopy (TOF-SIMS) profiles of STO(15nm)/$GdAlO_3$(15nm)/Si stacks as deposited and after RTA at 600°C in N_2. The good overlap between both profiles indicates no significant intermixing between the two layers is induced by annealing. The slight shift of the Al signal into the $SrTiO_3$ layer after anneal would suggest a very limited (if any) diffusion of Al in $SrTiO_3$. The good stability of the STO/$GdAlO_3$ bilayer was confirmed by x-ray reflectometry (XRR) measurements which show that the crystallization anneal has very little impact on the density of the $GdAlO_3$ layer (Tab.1). The higher density observed for $SrTiO_3$ is due to the crystallization.

3. Electrical evaluation

The electrical properties of the various stacks of interest ($SrTiO_3$ total thickness ~10nm) are presented in the following section. Based on the in-situ XRD results, $SrTiO_3$ films directly deposited on TiN (no seed) and STO/$GdAlO_3$/STO stacks were annealed at 600°C in N_2 while $SrTiO_3$ with seed approach were annealed at 450°C in O_2 (the seed anneal was done at 700°C in N_2). Pt top electrodes were deposited after crystallization anneal.
Fig.5 presents representative C-V curves measured on the stacks of interests. Relatively flat C-V characteristics with high capacitance densities (>35fF/cm^2) are observed for 10nm films. The slightly lower capacitance obtained for stacking approach is compensated by a superior capacitance vs. voltage behavior. The capacitance and conductance dependence upon capacitor area are shown on Fig.6 for the studied stacks. Relatively high dielectric constants could be extracted from the linear slope C vs. size (K~66 for $SrTiO_3$ directly on TiN; K~51 for $SrTiO_3$ with seed layer; K~42 for STO/$GdAlO_3$/STO) and combined with low conductance. The influence of the stacking approaches on the leakage properties of 10nm $SrTiO_3$ based capacitors with TiN bottom electrode is depicted in Fig.7. Clearly, using a seed layer or a multistack approach leads to significant reduction in leakage; the IV curve being quite symetric. Jg as low as 1.7×10^{-7} A/cm^2 (2.8×10^{-7} A/cm^2 and 6.2×10^{-7} A/cm^2) were obtained at ±0.8V when using the seed layer (STO/$GdAlO_3$/STO multistack) approach.

4. Conclusion

Stacking approaches (*i.e.* seed layer and multistack STO/$GdAlO_3$/STO) were compared to standard deposition of stoichiometric $SrTiO_3$ directly on TiN. Optimized stacks are proven to be efficient for leakage reduction while keeping high dielectric performances even for thin layers (~10nm). The seed layer approach presents the advantage of lowering the crystallization T of the bulk $SrTiO_3$ making possible the use of O_2 crystallization anneal when using non-noble metal electrodes like TiN. This leads to excellent leakage densities (1.7×10^{-7} A/cm^2 at ±0.8V) and high capacitance properties ($C_{density}$~45fF/μm^2). Such stacking approaches are of high interest in view of leakage reductions for next DRAM MIMCAP nodes.

References

[1] N. Menou *et al.*, Tech. dig. IEDM. **2008**, 929.
[2] M. Popovici *et al.*, submitted to J. Electrochem. Soc.
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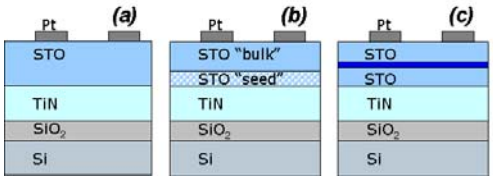

Fig. 1: Scheme of the studied $SrTiO_3$ based stacks. (a) STO deposited directly on TiN; (b) STO deposited on a seed layer (few nm) that is crystallized at 700°C in N_2; (c) Multistack STO/$GdAlO_3$/STO with $GdAlO_3$ thickness ~1nm

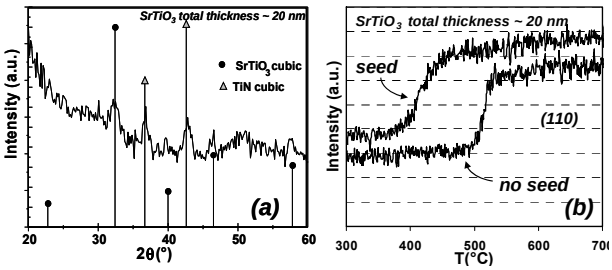

Fig. 3: (a) θ-2θscan of a 15nm $SrTiO_3$ film as deposited on a STO seed layer (~5nm) annealed at 700°C in N_2. The small STO peaks suggest that the seed layer is crystalline while the rest of the film is amorphous; (b) Intensity of the STO (110) peak as a function of T for STO films with and without seed layer measured by IS-XRD. Crystallization occurs at lower temperature when a seed layer is used.

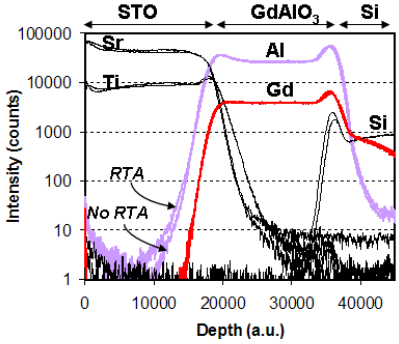

Fig.4: TOFSIMS profiles of STO/$GdAlO_3$/Si stacks as deposited and after RTA at 600°C in N_2. Overall no major change is observed. Only a slight shift of the Al signal into the STO layer after anneal would suggest a very small (if any) diffusion of Al in STO.

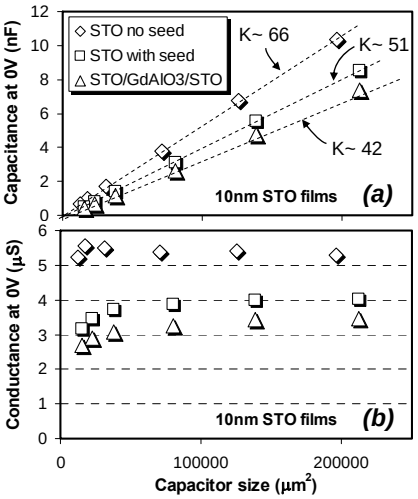

Fig.6: C (a) and G (b) area scaling for crystalline 10nm $SrTiO_3$ stacks deposited on TiN (top electrode is Pt). K values of the different stacks are extracted from the slope C vs. size.

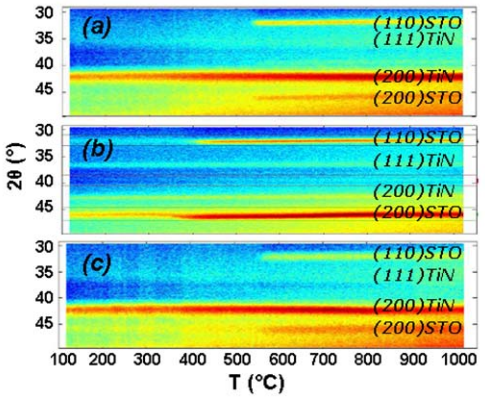

Fig. 2: In-situ XRD (0.2°C/s ramp, He) study of crystallization of thin ALD STO films (15-20 nm) on TiN. (a) $SrTiO_3$ deposited directly on TiN; (b) Seed layer approach; (c) STO/$GdAlO_3$/STO stacks. The temperature at which the STO layer crystallizes into the high-k perovskite structure depends on the stack.

	As deposited		After RTA 600°C	
	Thick. (nm)	*Density(%)*	*Thick. (nm)*	*Density(%)*
$GdAlO_3$	15.4	70.0	14.1	71.6
$SrTiO_3$	15.0	70.7	13.9	89.4

Tab. 1: Thicknesses and densities extracted from XRR measurements done on STO(15nm)/$GdAlO_3$(15nm)/Si stacks as deposited and after RTA at 600°C in N_2. No significant change is seen on the $GdAlO_3$ properties suggesting no intermixing with $SrTiO_3$.

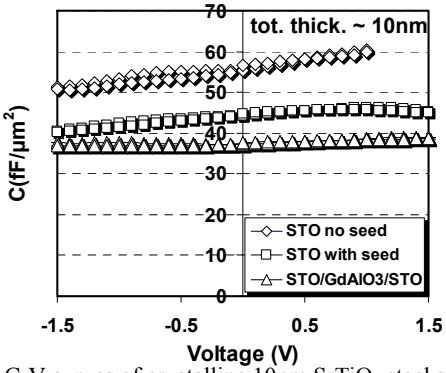

Fig.5: C-V curves of crystalline 10nm $SrTiO_3$ stacks deposited on TiN (top electrode is Pt). Crystallization anneals were done by RTA for 60 sec.: at 600°C in N_2 for STO without seed and for STO/$GdAlO_3$/STO stacks; at 450°C in O_2 for STO with seed layer.

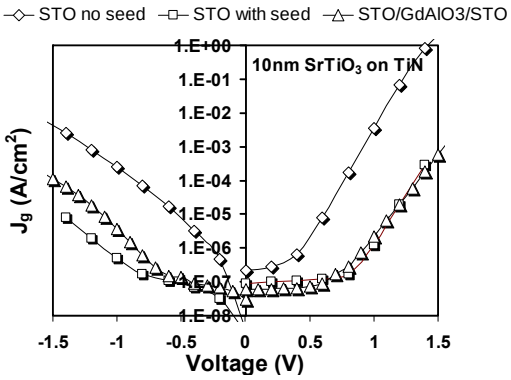

Fig.7: I-V curves of crystalline 10nm $SrTiO_3$ stacks deposited on TiN (top electrode is Pt). The step delay time was 550ms. Strong leakage reduction is observed when using a stack approach (seed or multilayer).