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Electrical defects in dielectrics for flash memories studied by Trap Spectroscopy by Charge Injection and Sensing (TSCIS)

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Introduction and purpose

In the field of non-volatile memory concepts, the TANOS (TaN(or TiN)/Al_2O_3/Si_3N_4/SiO_2/Si) gate stack has attracted considerable interest. For optimizing charge storage in the nitride layer and, simultaneously, optimizing the Al_2O_3 blocking layer, detailed information on the energy and spatial distribution of electronic defects in both layers is required. This information can be derived indirectly from modelling program/erase and reliability characteristics. However, this requires carefully chosen assumptions and fitting parameters.

Recently [1], we demonstrated how Trap Spectroscopy by Charge Injection and Sensing (TSCIS) can directly provide quantitative data on trap energy and spatial position in dielectrics. These data complement the memory device characteristics and improve our understanding of device operation and reliability. In this paper, the working principle of TSCIS, together with a number of examples on materials selected for use in memory applications, are described.

Measurement methodology

The principle of TSCIS is illustrated in Fig. 1. On the gate of an nmos transistor, V_{charge} ($>V_{th}$) is applied during time intervals with increasing length starting from ~10 ms up to 1000s. During this time, traps inside the bulk of the gate dielectric are charged by *direct tunnelling* of electrons from the inversion layer (Fig. 1b). In between the charging intervals, the gate voltage is switched for ~3ms to V_{sense} (with $0<V_{sense}<V_{th}$) and the source-to-drain current I_{SD} (with V_D=0.1V) is measured (Fig. 1c). The drop of I_{SD} at V_{sense} is converted into the V_{th}-shift using an initially measured I_{SD}-V_G characteristic (Fig. 1d). This measurement methodology has been modified from and is similar to fast V_{th}-evaluation methods developed for minimizing the relaxation during NBTI tests, and uses the same equipment and software [2].

After discharging the sample, V_{ch} is incremented and the sample is again charged. The final result (Fig. 2) shows the V_{th}-shift vs. t_{ch} measured for a range of V_{ch}-values.

Analysis

The data in Fig. 2 are transformed into a trap density profile following the algorithm schematized in Fig. 3. This calculation involves WKB-approximation for determination of the tunnelling distance, a Poisson solver for finding the band bending in the presence of an arbitrary charge profile and an algorithm to keep the detailed balance between the electron injection level and trapped charge.

The details of this calculation are not elaborated here, but the interpretation is schematically shown in Fig. 4a for the example of an SiO_2/Al_2O_3 stack in the presence of an Al_2O_3 defect band. By increasing t_{ch} at each V_{ch}, a trajectory in the dielectric band diagram is defined by the 1st subband energy level in the inversion layer at the corresponding tunnel distance. At low V_{ch}, the trajectory encompasses only deep traps close to the interface, and with increasing V_{ch}, the trajectory moves closer to the conduction band edge and further away from the interface, allowing shallow states to be occupied by injected electrons.

The defect band causes, as shown in Fig. 4b and c, (1) no V_{th}-shift as long as the trajectory stays below the band, (2) V_{th}-shift vs $\log(t_{ch})$ when the defect band is occupied by electrons, (3) saturation of the V_{th}-shift once the trajectory is above the defect band. When the complete data set of Fig. 2 is analysed, we can plot defect density vs. trap position and energy (Fig. 5a). We observe the defect band between ~1.7 and 2.0 eV below the Al_2O_3 conduction band edge.

Application

We have applied TSCIS to a variety of materials, each deposited on ~1 nm SiO_2 interface layer, that separates the substrate from the layer under study. With thicker SiO_2, too long t_{ch} is required for electrons to tunnel to the high-k dielectric.

Al_2O_3: Crystalline Al_2O_3 has a typical defect band, already shown in Fig. 5a. Depending on the processing details, the trap density can vary strongly. We have independently modelled the retention behaviour in written and erased state of a floating gate memory with Al_2O_3 interpoly dielectric (IPD) [3]. This required the presence of an Al_2O_3 defect band with identical energy level and trap density, confirming the consistency of our results.

In amorphous Al_2O_3 (with PDA @ 700C instead of 1000C) no distinct defect band signature is seen (Fig. 5b). Instead, all trap energy levels are equally present.

Si_3N_4: Fig. 6a shows the trap distribution in LPCVD Si_3N_4. We observe a peak concentration of traps at ~1.65eV below the nitride conduction band edge. Furthermore, the trap concentration increases towards the center of the nitride layer. Fig. 6b illustrates how a variation of the processing conditions affects the trap density spectrum. N-rich Si_3N_4 has the most sharply defined density peak, while O-rich or Si-rich recipes result in either very low or very high trap density distributed over a wide energy range. The TSCIS data are consistent with retention modeling as will be shown in detail in a future publication.

Other materials: In [1], we demonstrated that TSCIS has sufficient resolution to detect the low (~10^{17} cm^{-3}) trap density in high-quality SiO_2 after stress. The TSCIS results again agree with previous studies on flash retention.

Furthermore, TSCIS is a powerful tool to study the defect properties in alternative dielectrics and timely understand their properties. As an example, we present in [4] several processing options of HfAlO as potential IPD. Future publications on GdScO, DyScO, LuAlO, and many more materials are being prepared.

Conclusions

Trap Spectroscopy by Charge Injection and Sensing (TSCIS) is a fast and powerful material analysis technique that provides detailed information on the trap density profile and trap energy level in dielectric materials. It has excellent resolution and is capable of distinguishing between different process-variations. These data help to understanding the operation and reliability of memory devices and facilitate a screening of new dielectric materials.

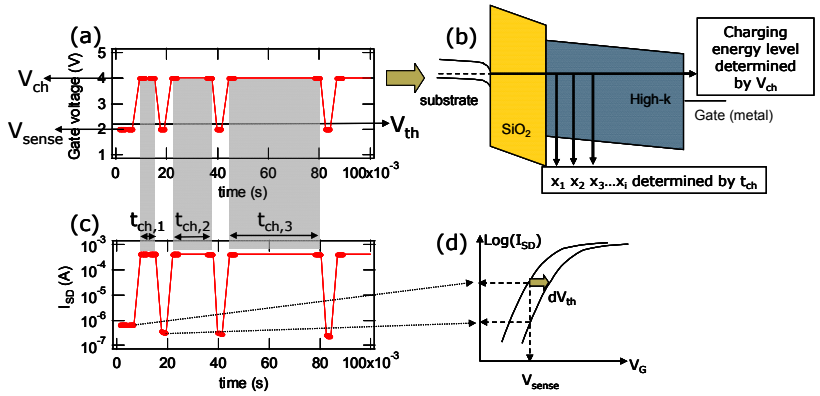

Fig. 1: The principle of Trap Spectroscopy by Charge Injection and Sensing (TSCIS). By applying $V_{ch}>V_{th}$ at the gate of an nmos transistor (Fig. a), the dielectric traps are charged by direct tunnelling from the inversion layer (Fig. b). In order to measure the trapped charge density, the change of the source-drain current (with V_D=0.1V) is measured at V_{sense} (Fig. c). The interruptions at V_{sense} are short (~3ms), such that all charge sufficiently far away from the interface remains in the dielectric. The change of I_{SD} is converted to a V_{th}-shift using an initially measured I_{SD}-V_G characteristic (Fig. d).

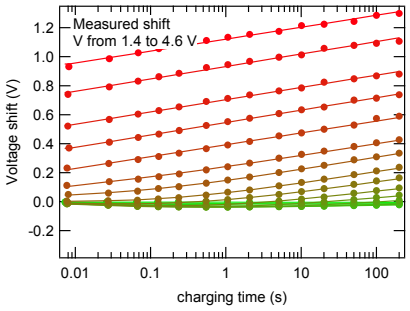

Fig. 2: A typical TSCIS result showing the V_{th}-shift as a function of t_{ch} for increasing V_{ch}. In this case V_{ch} varied from 1.4 to 4.6 V in steps of 0.2 V. The data are obtained on a structure with IMEC clean (=~0.9 nm SiO_2) / 10 nm ALD Al_2O_3 + PDA@1000C, 60".

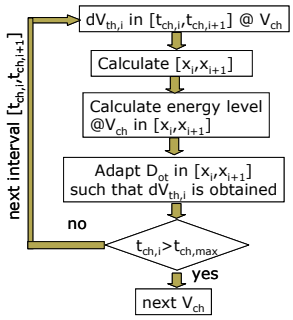

Fig. 3: Simplified flow of the analysis algorithm. Each t_{ch}-interval corresponds to an *x* interval (with x defined in Fig. 4), calculated using WKB-direct tunnelling approximation. In this *x*-interval, V_{ch} together with the trapped charge density determine the energy level up to which traps can be filled. Next, the trap density in the energy/distance space is adapted such that the measured V_{th}-shift is obtained. At each moment in the calculation, the charge-induced conduction band bending and corresponding change of the tunnel distance are accounted for.

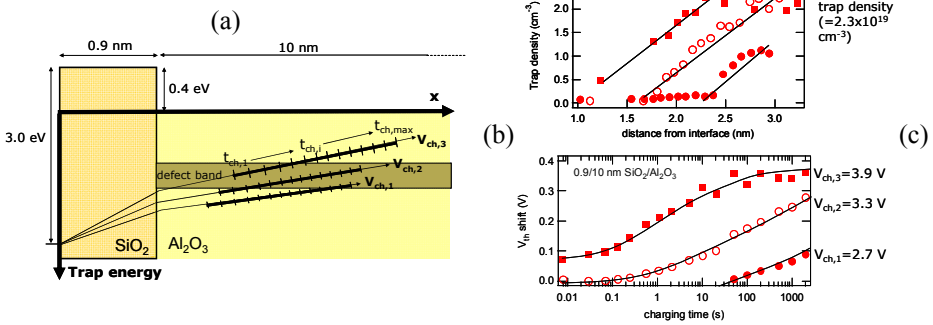

Fig. 4: (a) Schematic explanation on how a defect band in Al_2O_3 is sensed by TSCIS. At each V_{ch}, a sweep from $t_{ch,1}$ to $t_{ch,max}$ projects a trajectory in the dielectric band diagram.
Fig. (b) shows selected V_{th}-t_{ch} traces and Fig. (c) the calculated trap densities, corresponding with the three trajectories in Fig. (a). At low $V_{ch,1}$, the defect band is only sensed at long t_{ch} (bottom curves in Fig 4 b and c). At intermediate $V_{ch,2}$, the band is sensed from short t_{ch} on (middle curve in Fig. 4b and c) until it reaches the top of the band at $t_{ch,\,max}$. At high $V_{ch,3}$, traps are already occupied at the minimal $t_{ch,1}$ and when the trajectory leaves the defect band, the V_{th}-t_{ch} trace levels off (top curve in Fig. 4b and c). After analysis, the defect density is in this example is 2.3x10^{19} traps/cm^3.

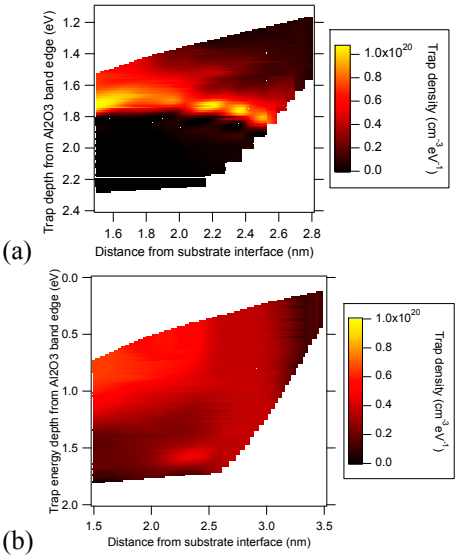

Fig. 5: The trap density spectrum of Al_2O_3. Fig 5(a) shows crystalline material with a defect band (data of Fig. 2 after analysis). Fig.5(b) shows amorphous Al_2O_3 (stack = 1 nm ISSG SiO_2 / 12 nm ALD Al_2O_3 + PDA@700C in N_2, 60"). In amorphous material no distinct features are seen and in the scanned range, traps are distributed evenly in both space and energy.

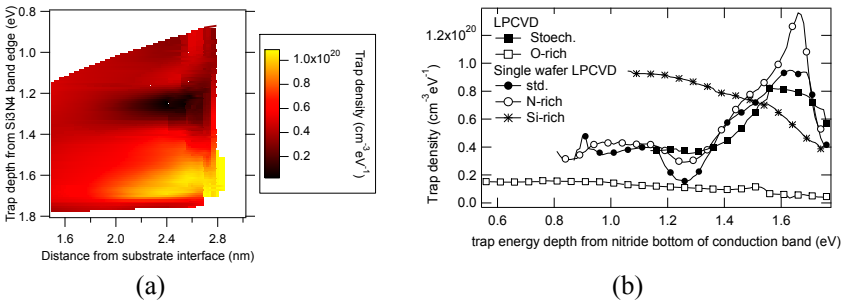

Fig. 6(a): The trap density spectrum of single wafer LPCVD Si_3N_4. (stack = 1 nm ISSG SiO_2 / 6 nm nitride / 10 nm ALD Al_2O_3 + PDA@1100C in O_2). Fig. 6(b): The average trap density profile vs. energy in the scanned range at 2 to 2.9 nm from the substrate. Five differently processed nitrides are considered. Three gives comparable trap density profiles with maximum at ~1.6-1.7 eV below the conduction band edge. The Si-rich sample shows a huge increase of the shallow trap density. In the O-rich recipe, the trap density is strongly reduced, possibly due to the formation of oxynitride.

References:

[1] R. Degraeve et al., IEDM 2008.
[2] B. Kaczer et al., IRPS 2008.
[3] B. Govoreanu et al., IEDM 2008.
[4] B. Govoreanu et al., presented at INFOS 2009.