# Charge Localization During Program and Retention in NROM-like Nonvolatile Memory Devices

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### 1. Introduction

An alternative solution to standard Flash memories is represented by nitride-trap memories as SONOS or NROM memories. NROM in particular can be operated in 2-bit/cell mode using localized trapping in Si<sub>3</sub>N<sub>4</sub> film [1]. Therefore it can comply with the increasing demand of bit density. However these structures are facing retention issues at high temperature and a quantitative analysis of the charge distribution during program and retention is required.

Various techniques have been employed to deduce the distribution of trapped charges injected by channel hot electrons in the Oxide/Nitride/Oxide stack (ONO) of standard NROM devices. Among them we find charge pumping technique [2], GIDL and substhreshold slope monitoring [3], or analyses based on the surface potential model [4] and the measure of reverse/forward programming windows  $(\Delta V_t R / \Delta V_t F;$  Fig. 1). In this work the method described in [4] will be used on experimental data in order to evaluate the trapped charge distribution in program and retention conditions. The lateral migration (i.e. inside the trapping layer) and vertical migration (i.e. charge loss) of the trapped charges during retention will be quantitatively evaluated. Other trapping layers such as Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> are also investigated.

## 2. Samples Description and Methodology

The devices under analysis are presented on Fig.2. The gate stack is composed by 5 nm tunnel SiO2 plus 6 nm charge trapping layers: Si<sub>3</sub>N<sub>4</sub> deposited by LPCVD or HfO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> deposited by ALCVD at 350°C. Then, a 10 nm thick High Temperature Oxide (HTO) is deposited as top oxide plus N+ Si-poly gate. After gate etching, standard processing steps include NiSi silicidation. Using the method presented in [4], the charge density  $Q_{density}$  and the effective charged length  $L_{charged}$  are extracted (Fig.3), based on  $\Delta V_t R$  and  $\Delta V_t F$  measured during program and retention.

## 3. Results and Discussions

*Programming dynamics* - Fig. 4 shows that the programming dynamics are dependent on the trapping layers and this even for short programming pulses, as shown in [6]. However, as shown in Fig. 5 the location of the charge is independent of the material: indeed  $L_{charged}$  is equal to 40 nm for  $Q_{density}$  smaller than  $10^{13}$  cm<sup>-2</sup> (stress time of the order of 0.01 s). This can be explained by the fact that all devices have the same junction profile thus they have identical injection efficiency of accelerated carriers by the electric field [3]. Then when  $Q_{density}$  reaches  $1.4 \times 10^{13}$  cm<sup>-2</sup> (stress time over 0.01 s),  $\Delta V_t R$  continue to increase (Fig. 4) due to the increase of  $L_{charged}$  (Fig. 5). Seemingly the traps

over drain junction becomes saturated, thus newly injected charges can redistribute in the trapping layer farther from the junction. We conclude that the charge distribution behavior during programming is similar for the three materials, even if the device with  $Si_3N_4$  shows the best capture efficiency during the programming dynamics.

Retention and model - Fig. 7 shows data retention characteristics of devices at 25°C and 125°C. In Fig. 8, the extraction of  $Q_{density}$  and  $L_{charged}$  shows that the  $\Delta V_t R$  shift is only due to the lateral charge migration at low temperature (excepted for Al<sub>2</sub>O<sub>3</sub> at 125°C, where the vertical charge loss is the dominant mechanism). We stress that at high temperature (200°C)  $\Delta VtR$  decreases mainly because of vertical electron loss (not shown here). To simulate the lateral migration of the trapped charges the numerical resolution of 1D Drift-Diffusion system is adopted (Fig. 9-10). From Fig. 11 we notice that the diffusion process is negligible with respect to drift, and the drift of charged particles is found equal to  $L_{charged} = L_{charged0} + Aln(t)$  (Fig. 11) with A linearly dependent with  $\mu_{eff}Q_{total}/\varepsilon_r\varepsilon_0$  and independent of the shape of the injected charge.  $\mu_{eff}$  corresponds to an effective mobility that includes the trap/detrap process plus the drift in the conduction band [7]. Fig. 12 quantifies the lateral migration of trapped charges  $L_{charged}$  for Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub>. The lateral migration follows a logarithmic law and the lowest drift is observed for Si<sub>3</sub>N<sub>4</sub>.

#### 4. Conclusions

In this paper, we have quantified the localization of the charges during programming and retention in NROM-like devices, based on experimental measurements (in particular of  $\Delta V_t R$  and  $\Delta V_t F$ ) and a surface potential model [4]. It appears that during programming the charge is injected on a 40nm-length region in the trapping layer, with a charge density up to  $1.4 \times 10^{13}$  cm<sup>-2</sup>. Then the injected charge density saturates and the trapped charge region broadens. During retention, the lateral migration of the charge appears to be the dominant mechanism of the  $V_t$  shift at room temperature. We have been able to quantify this shift based on a 1D drift model (diffusion being negligible).

#### References

- [1] B. Eitan et al, IEEE EDL, vol. 21, n°11, 2000, pp. 543-545.
- [2] A. Furnemont et al, Proc. IEEE NVSMW, pp. 66-67, 2006.
- [3] E. Lusky et al, IEEE TED, Vol. 51, No. 3, 2004, pp.444-451.
- [4] L. Perniola et al, IEEE IEDM Tech. Dig., 2005, pp. 857-860.
- [5] A. Furnemont et al., IEEE IEDM Tech. Dig., 2006.
- [6] T.Sugizaki et al., VLSI Tech Dig., 2003, pp.27-28.
- [7] E.Vianello et al., ESSDERC, 2008, pp. 107-110.



Fig. 1:  $\Delta V_t R$  ( $\Delta V_t F$ ) is the programming window in reverse (forward) read condition.



Fig. 4:  $\Delta V_t R$  dynamics as a function of stress time for virgin devices. Stress parameters V<sub>G</sub>=10 V, V<sub>D</sub>=5 V, V<sub>S</sub>=V<sub>B</sub>=0 V.



Fig 7:  $\Delta V_t R$  evolution at 25°C and 125°C during retention for Si<sub>3</sub>N<sub>4</sub>, Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> trapping layers.



Fig.10: Explanation of 1D model used to model the lateral migration of the charge. Shapes 1 & 2 are used as initial conditions for simulations of Fig. 11.

	D1	D2	D3
Tunnel	SiO <sub>2</sub>		
Oxide	5nm		
Trapping	$Si_3N_4$	HfO <sub>2</sub>	$Al_2O_3$
layer	6nm	6nm	6nm
Тор	HTO		
Oxide	10nm		

Fig. 2: Devices under analysis. The devices are 10  $\mu$ m large and 350 nm long.



Fig. 5: Extracted  $Q_{density}$  and  $L_{charged}$  as a function of time from the dynamics of Fig. 4.



Fig. 8: Total charge variation in the trapping layer  $Q_{density} \propto L_{charged}$  extracted dur-



Fig. 11: Numerical resolution of the 1D Drift-Diffusion equations. To note that we obtain a perfect fit with a law equal to  $L_{charged} = L_{charged0} + Aln(t)$ 



Fig. 3:  $Q_{density}$  and  $L_{charged}$  as described in [4]. The total charge trapped in the stack is equal to  $Q_{density} \ge L_{charged}$ .



Fig. 6:  $Q_{density}$  as a function of  $L_{charged}$ extracted from the dynamics of Fig. 4.  $V_G=10 V \& 12 V, V_D=5V, V_S=V_B=0V.$ 



Fig. 9: 1D Drift-Diffusion equation and approximations to a perfect diffusion or drift process.



Fig. 12:  $L_{charged}$  extracted during retention (Fig. 7) at 25°C for Si<sub>3</sub>N<sub>4</sub>, Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> trapping layers. A is in nm/s.