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Study of Transient Tunneling Current and Charge-Trapping Behaviors of SONOS-type Devices Using Pulse-*IV* Technique

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I. Introduction

Pulse-*IV* techniques have been widely used to characterize traps in high-K gate dielectric of CMOS logic devices [1-3]. The conventional pulse-*IV* technique for high-K gate dielectric mainly deals with drain current transient response and fast NBTI behavior. In this work, we developed a special operation mode, where the current is characterized concurrently with the applied pulses. Therefore, the corresponding transient gate tunneling current of various SONOS-type devices can be accurately monitored. Using this new technique, the charge tunneling and trapping behaviors of various SONOS-type devices have been investigated exhaustively. In this work, we also proposed a theoretical model to simulate transient gate tunneling current of SONOS-type devices.

II. Sample Descriptions and Pulse-*IV* setup

Table 1 lists various SONOS-type devices studied in this work. Large area (500μm × 500μm) capacitors (n^+ source/drain, p-well, and p^+ poly gate) are fabricated to provide enough gate tunneling current (> 1μA). Figure 1 shows the pulse-*IV* setup used in this work. The pulse is applied to gate (V_G) while the drain, source, and body are connected together to measure the gate tunneling current (I_G). (Capacitors in this study are fabricated with source/drain and body contacts.) The I_G is converted to voltage signal by using a fast current to voltage amplifier. The oscilloscope can simultaneously collect the V_G and I_G waveforms.

Cable connection, shielding and impedance matching are carefully arranged to eliminate spurious response.

III. Results and Discussion

(a) Transient Gate Tunneling Current of SOS:

We first measured transient gate tunneling current of SOS (S1, O = 25Å) for a reference and calibration, as illustrated in Fig. 2. Since this standard gate oxide capacitor does not have any trapping layer, ideally, its I_G should be very stable under a steady bias. The results in Fig. 2 show no spurious response for various V_G and pulse widths when the V_G is kept constant. This indicates that our setup does not generate detectable noise, and the gate current response under a steady V_G is reliable.

(b) Transient Gate Tunneling Current of SNOS:

Next, we measured the transient gate tunneling current of SNOS (S2, NO = 60/75Å, SONOS without B.O.), as shown in Fig. 3.

It should be mentioned that during the rising/falling periods of V_G pulse there may be some spurious response, and thus we do not study gate transient current in those periods.

Under steady $+V_G$ (Fig. 3(a)(b)) the I_G (mainly contributed by the electrons from channel) rises initially but then drops sharply and decreases to almost zero. Moreover, this transient behavior is independent of pulse width and similar for different V_G, implying that this current response is indeed the real transient behavior instead of spurious response. The decreased I_G during programming time is easily understood since when electrons are trapped in nitride, the built-in electric field suppresses the tunneling current. On the other hand, under $-V_G$ (Fig. 3(c)(d)) the transient characteristics behave differently, and I_G gradually increases and then saturates. Again, this transient behavior is insensitive to V_G and pulse width. Even though there is no B.O., we still expect the I_G mainly comes from electron tunneling from the gate. On the other hand, because there is substantial hole injection from channel (since nitride has smaller hole barrier height ~ 2eV), some hole trapping occurs. This hole trapping enhances the electron tunneling and in turn increases I_G. The saturation current is different for $+V_G$ (~ 0A for +20V) and $-V_G$ (~ 0.7mA for –16V). Under $+V_G$ the T.O. in SNOS can suppress the trapped electron out-tunneling/gate hole injection and this results in lower current. However, under $-V_G$ since there is no B.O. that can block the trapped electron out-tunneling/channel hole injection, resulting in higher gate injection and larger saturation current.

(c) Transient Gate Tunneling Current of SoNOS:

The transient gate tunneling currents of SoNOS (S3, oNO = 25/70/62Å) under $+V_G$ and $-V_G$ are shown in Fig. 4(a) and (b), respectively. Since SoNOS has both T.O. and B.O. that can prevent out-tunneling or de-trapping, the injected electrons accumulate in the nitride and the decreased electric field causes sharply decreased I_G. The corresponding CV curves after $+/-V_G$ are also shown in Fig. 4(c) and (d), respectively. The V_{FB} shift of $+V_G$ (~ 6V) is much larger than that of $-V_G$ (~ 1.65V) since the thicker T.O. blocks trapped electron out-tunneling and external hole injection more efficiently, and the n^+ source/drain can provide more electrons than p^+ poly gate. Moreover, these trapped electrons will further suppress the electron injection in the second gate pulse (2^{nd} injection); therefore, the I_G stays near zero (Fig. 4(a)(b)), and the V_{FB} shifts are very small (Fig. 4(c)(d)).

(d) Transient Gate Tunneling Current of SONOS:

The transient gate tunneling current of SONOS (S4, ONO = 54/70/90Å) under $+V_G$ is shown in Fig. 5(a). Similar to SoNOS, the I_G decreases with time. Previously, we have shown that SONOS with thicker nitride (>70Å) exhibits full-capturing characteristics [5]. Therefore, we used the theoretical model (based on the fully captured assumption) shown in Table 2 to simulate the transient behavior of S4. Figure 5(a) shows that the experimental I_G can be well fitted by using reasonable parameters (Φ_B = 3.1eV and m_{ox} = $0.5m_0$). This result further supports that SONOS with sufficient nitride thickness indeed can capture all the injected electrons. Figure 5(b) shows that the V_{FB} shift is very large.

(e) Transient Gate Tunneling Current of BE-SONOS:

The transient gate tunneling currents of BE-SONOS (S5, 13/20/25/70/90Å) under $+V_G$ and $-V_G$ are shown in Fig. 6(a) and (b), respectively. Under $+V_G$ operation, the channel electrons can tunnel through the ONO barrier, and then are trapped in the nitride, which causes decreased I_G and large V_{FB} shift (Fig. 6(c)). Using the similar parameters as SONOS, the transient behavior can be also well-fitted by our theoretical model, as shown in Fig. 6(a). Therefore, BE-SONOS also fully captures electrons like SONOS. On the other hand, under high $-V_G$ operation electrons inject from the gate and holes from channel simultaneously, and I_G stays high because electrons and holes annihilate each other and there is no accumulation of charge to reduce the electric field. Moreover, under the right conditions (–22V) the electron current and the hole current reach balance (erase saturation), and the V_{FB} stays unchanged (Fig. 6(d)). A second $-V_G$ pulse produces the same I_G and V_{FB} behavior because e/h continue to annihilate each other.

IV. Summary

The complex transient gate tunneling current and charge- trapping behaviors of various SONOS-type devices are characterized and modeled.

References:

[1] B. H. Lee, *et al*, IEDM, pp. 859-862, 2004.
[2] G. Bersuker, *et al*, APL, v. 87, pp. 042905(1-3), 2005.
[3] C. D. Young, *et al*, IRPS, pp. 75-79, 2005.
[4] H. T. Lue, *et al*, T-ED, pp. 2218-2228, 2008.
[5] H. T. Lue, *et al*, IRPS, pp. 177-183, 2007.

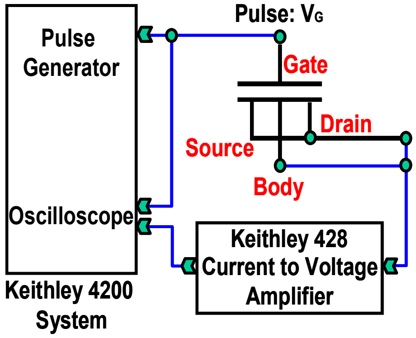

Fig. 1 Pulse-*IV* setup for transient gate tunneling current measurement. Pulse is only applied to the gate while source/drain and body are connected together to measure the gate current by a current-to-voltage amplifier. Both gate pulse and current can be monitored simultaneously by oscilloscope.

	S1	S2	S3	S4	S5
B.O. (Å)	25	NA	25	54	13/20/25
N (Å)	NA	60	70	70	60
T.O. (Å)	NA	75	62	90	75
Structure	SOS	SNOS	SoNOS	SONOS	BE-SONOS

Table 1 Sample descriptions. Various SONOS-type devices are fabricated. The device is a large-area NMOSFET with source/drain, with P^+-poly gate in order to suppress gate injection during –FN.

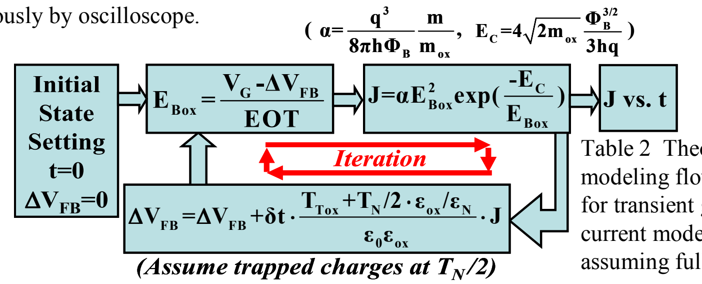

Table 2 Theoretical modeling flow chart for transient gate current modeling by assuming full capture.

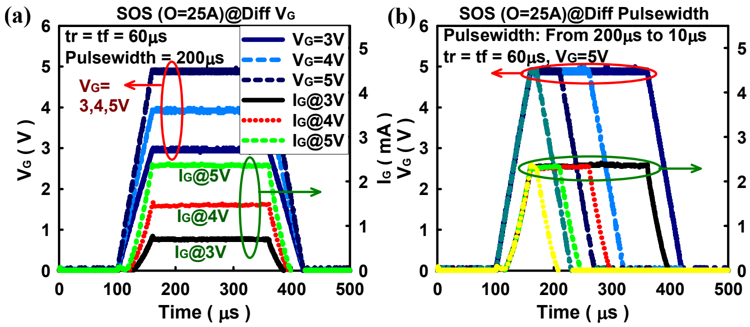

Fig. 2 Transient gate current of SOS (S1) under various (a) gate voltages and (b) pulse widths. The I_G stays constant, and there is no transient relaxation for a pure gate oxide. This indicates that our measurement setup does not have spurious response.

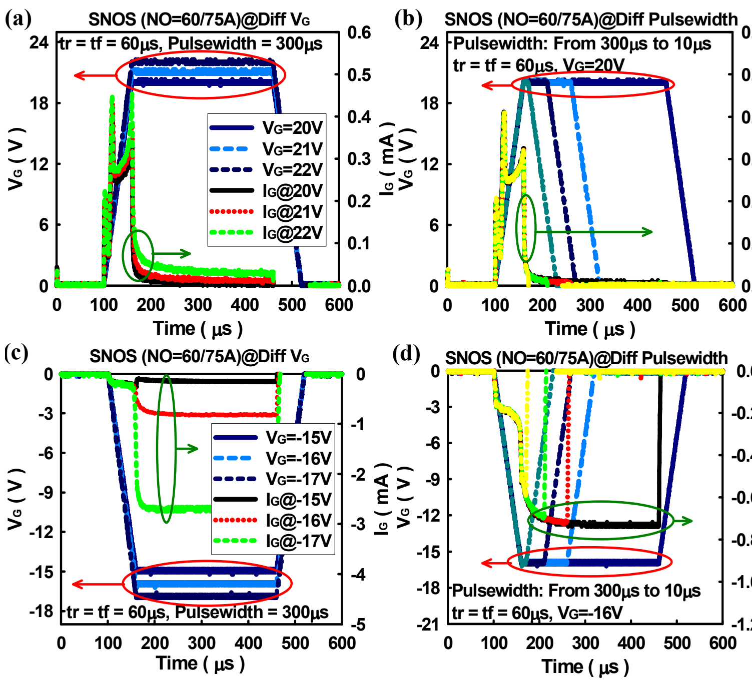

Fig. 3 Transient gate current of SNOS (S2) under various V_G: (a) different $+V_G$. (b) different pulse widths. The I_G (electrons from channel) drops rapidly to very low level (near zero) due to electron trapping. (c) Transient gate current under various $-V_G$, (d) different pulse widths. The I_G (electrons from gate) rises during the $-V_G$ pulse. This indicates that there is some hole trapping (coming from channel) that helps increase the electron tunneling.

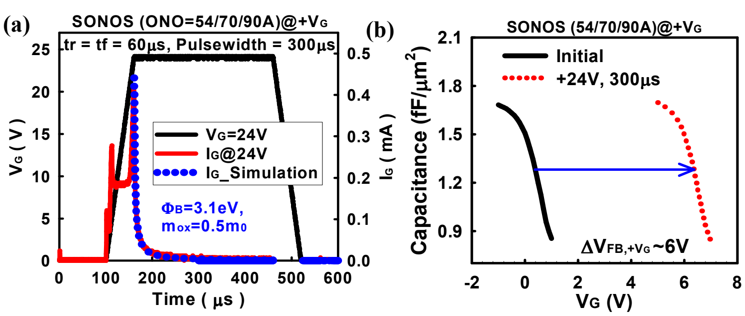

Fig. 5 (a) Transient gate current of SONOS (S4) under $+V_G$. The measured I_G can be well fitted with our model when 100% capture is assumed. The I_G behavior is similar to Fig. 3(a). (b) CV curves after $+V_G$ programming. The injected electrons can be fully captured by nitride, leading to a large V_{FB} shift.

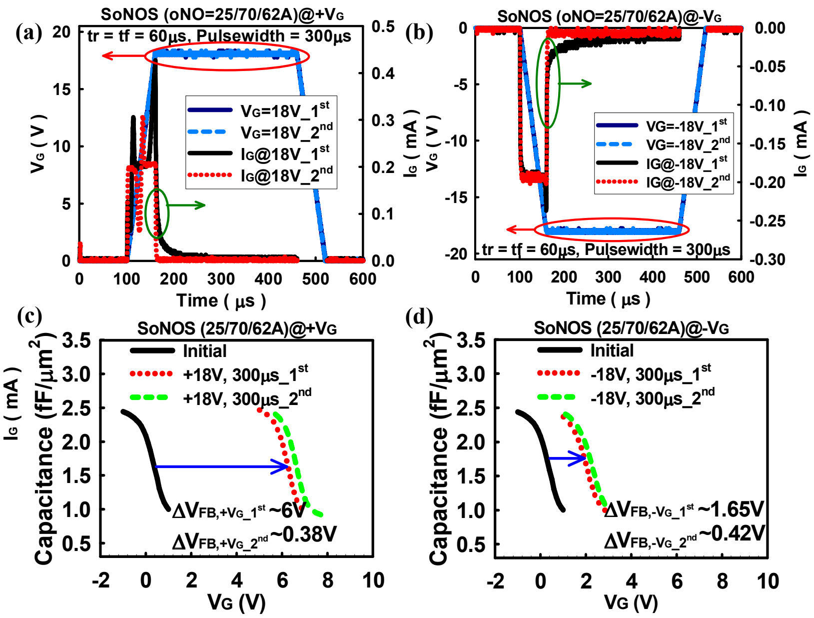

Fig. 4 Transient gate current of SoNOS (S3) under (a) $+V_G$ and (b) $-V_G$. The trapped electrons cause sharply decreased I_G and suppress the tunneling current in the second gate pulse (2^{nd}). The corresponding CV curves after (c) $+V_G$ and (d) $-V_G$ pulses. The V_{FB} shift of $+V_G$ is much larger than that of $-V_G$, and the V_{FB} shifts in the second gate pulses are very small.

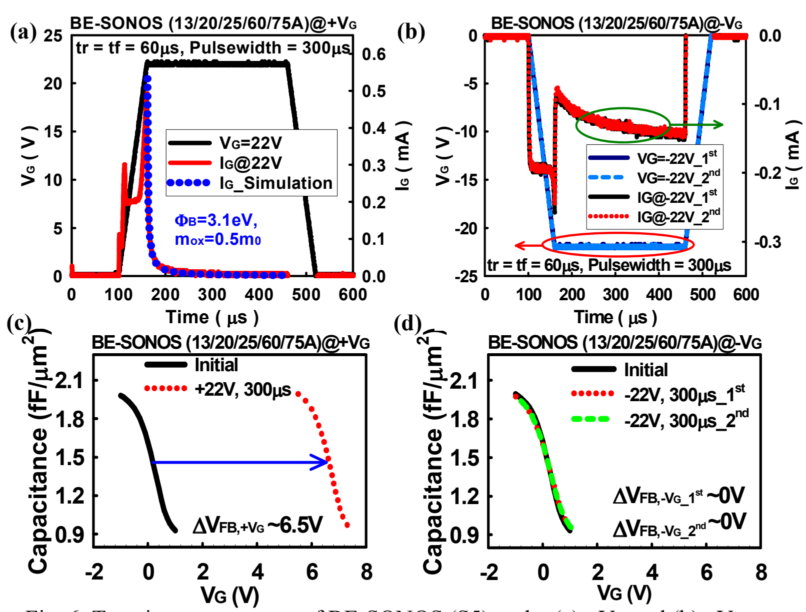

Fig. 6 Transient gate current of BE-SONOS (S5) under (a) $+V_G$ and (b) $-V_G$. Under $+V_G$ the trapped electrons cause a rapid drop of I_G (electrons from channel) and large V_{FB} shift ((c)). However, under $-V_G$ the trapped holes cause increased I_G (electrons from gate). A balance of electrons and holes is reached, and the V_{FB} shift is very small ((d)). The second pulse simply repeats the same behavior.