Roles of Traps Generated in $\text{Al}_2\text{O}_3$ Film with respect to Memory Characteristics in MANOS

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Introduction

Coupling interference from adjacent cells is one of the key issues in further scaling of floating-gate flash memories. Recently, charge-trap memories have been extensively studied in view of their immunity to the coupling interference. MANOS (Metal/$\text{Al}_2\text{O}_3$/SiN/$\text{SiO}_2$/Si) stacked structure is a commonly used charge-trap memory owing to its wide memory window and good retention characteristics [1, 2]. In this stack, it is generally believed that $\text{SiN}$ provides trap sites and $\text{Al}_2\text{O}_3$ blocks charge transfer between $\text{SiN}$ and gate electrode [1]. However, the stack without $\text{SiN}$ layer also showed memory characteristics [3, 4]. By comparing memory characteristics of stacks with and without $\text{SiN}$ trapping layer, we quantitatively confirmed for the first time that $\text{Al}_2\text{O}_3$ provides most of the traps. We also investigated effects of annealing on the trap characteristics of $\text{Al}_2\text{O}_3$ layer in detail. Moreover, we demonstrate a structure that simultaneously provides a sufficient amount of traps and good retention characteristics.

Experimental

Thin $\text{SiO}_2$ films (tunnel oxides) were thermally grown on n- and p-types of Si substrate. $\text{SiN}$ and $\text{Al}_2\text{O}_3$ films were subsequently deposited by CVD on the $\text{SiO}_2$. In some of the samples (MAOS: Metal/$\text{Al}_2\text{O}_3$/SiN/$\text{SiO}_2$/Si sub.), $\text{SiN}$ deposition was skipped [3]. TiN (10nm)/W (50nm)/TiN (10nm) of metal gate electrodes was formed. Several conditions of PGA (post-gate annealing) were applied in $\text{N}_2$ at 750°C~1000°C. MONOS (Metal/SiO$_2$/SiN/$\text{SiO}_2$/Si sub.) stack was separately prepared as a reference. Block $\text{SiO}_2$ was formed by HTO-CVD in this stack. All of the samples were finished by forming gas annealing at 400°C for 30min. Sample structures, annealing conditions, and abbreviations of the sample names are summarized in Table 1.

C-V and I-V characteristics were measured for these capacitors before and after program (positive-biased) and erase (negative-biased) operations. The effect of light irradiation was also examined for n-substrate (pMOS) capacitor to confirm the effect of hole injection from substrate in negative-biased conditions.

Results and Discussion

Fig.1 shows dependence of program/erase (P/E) bias on $V_{FB}$ shifts in MAOS and MANOS structures. Regardless of carrying out the PGA, almost the same amount of positive $V_{FB}$ shift was observed in MAOS as in MANOS, even though MAOS does not have special charge-trap layers such as $\text{SiN}$. This result indicates $\text{Al}_2\text{O}_3$ layer provides most of the electron trap sites in two of these stacked structures [3, 4]. In the case of erase operation, negative $V_{FB}$ shifts were observed both in MANOS and MAOS with PGA, whereas it was not observed without PGA. This is probably due to trapping of holes injected from substrate in hole trap sites generated in $\text{Al}_2\text{O}_3$ during PGA. Fig.2 shows an effect of light irradiation on erase characteristics of MANOS stacked pMOS capacitor with PGA. Negative $V_{FB}$ shift was observed only when erase operations were carried out with light irradiation, i.e. a sufficient number of holes were supplied from substrate. Positive $V_{FB}$ shifts due to reverse tunneling from gate electrodes were not observed in either case. Thus, we conclude that the negative $V_{FB}$ shifts under negative biased conditions are caused by trapping of holes injected from substrates. Then, to confirm where the hole trap sites are formed in these stacks, we compared the erase characteristics of MAOS, MANOS and MONOS for various PGA temperature. As shown in Fig.3, the negative $V_{FB}$ shifts were observed when $\text{Al}_2\text{O}_3$ films were inserted in the stacks (MAOS and MANOS). On the other hand, no negative $V_{FB}$ shifts were observed in MONOS. Moreover, negative $V_{FB}$ shifts increased as the annealing temperature increased. These results strongly suggest that the hole trap sites were not generated in $\text{SiN}$ and $\text{SiO}_2$, but generated in $\text{Al}_2\text{O}_3$ or at $\text{Al}_2\text{O}_3$/SiO$_2$ interface during PGA.

Changes of physical properties of $\text{Al}_2\text{O}_3$ by high-temperature annealing were also investigated. XRR, TEM and electron diffraction were carried out for various annealing conditions of $\text{Al}_2\text{O}_3$. As shown in Fig.4, density of $\text{Al}_2\text{O}_3$ was increased by annealing above 750°C. Fig.5 shows plan-view TEM images and electron diffractions taken from these samples. Crystallization of $\text{Al}_2\text{O}_3$ is clearly observed in 1000°C 0.1s and 750°C 3600s annealed samples. Changes in density indicated in Fig.4 are thought to be an effect of crystallization of $\text{Al}_2\text{O}_3$. Fig.6 shows the relationship between negative $V_{FB}$ shifts erased at $V_{th}$=−18V and density of $\text{Al}_2\text{O}_3$. The negative $V_{FB}$ shift clearly increases as the $\text{Al}_2\text{O}_3$ density increases. This indicates that generation of hole trap sites is related to $\text{Al}_2\text{O}_3$ crystallization.

Degradation of retention was also observed in high-temperature annealed samples, as shown in Fig.7. This is thought to be another effect of generation of the trap sites. For further analysis of the effect of trap sites on the retention characteristics, we investigated the temperature dependence of leakage current ($J_L$). Strong temperature dependence on $J_L$ was observed in the sample annealed at 900°C for 300s (Fig.8(b)), whereas only a slight dependence was observed in that annealed at 900°C for 0.1s (Fig.8(a)). Fig.9 shows activation energies ($\Delta E_a$), extracted from temperature dependence by using the relationship of $\Delta E_a = kT \ln (J_L/J_0)$, assuming PF emission. Four levels of $\Delta E_a$'s (0.12eV, 0.18eV, 0.21eV, and 0.25eV) were extracted in the case of 300s PGA. These defects, which formed electron leakage paths, were located at energy levels of 0.12−0.25eV below the bottom of conduction band of $\text{Al}_2\text{O}_3$. It might be noted that these defects closely related to the traps are essential for the memory characteristics themselves. In fact, there are some trade-off relationships between memory windows and retention characteristics as shown in Figures 6 and 7.

Finally we demonstrated a method for suppressing degradation of retention on the basis of the above understanding. An amorphous layer was inserted between $\text{Al}_2\text{O}_3$ and metal gate, as shown in Fig.10. It simultaneously enables elimination of leakage paths through blocking oxide and keeping of almost the same amount of electron or hole traps. A 10nm-thick Si-rich AlSiO$_x$ was deposited as the amorphous layer. Fig.11 shows comparison of P/E window between MANOS and $\text{Al}_2\text{O}_3$-inserted MANOS. There are no significant differences between the two stacks. Fig.12 shows a comparison of retention between MANOS and $\text{Al}_2\text{O}_3$-inserted MANOS. As expected, $\text{Al}_2\text{O}_3$-inserted MANOS shows excellent retention characteristics.

Conclusion

We have systematically investigated the impact of annealing process on generation of traps and defects in $\text{Al}_2\text{O}_3$ films, and revealed that traps and defects in $\text{Al}_2\text{O}_3$ induced by thermal process play an important role in realizing the memory characteristics of MANOS. Furthermore, we have demonstrated the improvement of retention by $\text{Al}_2\text{O}_3$-inserted MANOS.

References

Comparison of ∆Ea (eV) range of 750~1000 oC was performed for MAOS and MANOS. Annealing in the annealed Al2O3 with various conditions in 0.1s and 300s annealing at 900 oC.

Table 1 Fabricated stack structures in this work

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<tr>
<td><strong>MAOS</strong></td>
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<td>Metal</td>
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<td>Block Ox</td>
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<td>Charge trap</td>
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<td>Tunnel Ox</td>
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Post gate Annealing (PGA) in LP-N2

temperature | time
750~1000°C | 0.1~3600s

Fig. 1 Impact of PGA on P/E characteristics of MAOS and MANOS. PGA was performed at 900°C for 0.1s. Pulse times of program/erase are 50ms/pulse × 200times. Vtshifts are difference between Vt at fresh and Vt after P/E.

Fig. 6 Relationships between negative Vtshift by erasing at -18V and density of annealed Al2O3 with various conditions in MAOS and MANOS. Annealing in the range of 750~1000°C was performed for 0.1~3600s.

Fig. 7 Retention characteristics for different annealing times at 900°C PGA with MAOS and MANOS stack, showing the degradation of retention with PGA time increase. The initial storage charges by programming were made with 1x1017/cm2 in the stacks.

Fig. 9 Comparison of ∆E between 0.1s and 300s annealing at 900°C. ∆E’s were obtained from Fig.8 by using the relationship of ∆E = kTln(J/J0), assuming PF emission.

Fig. 10 Schematic illustration of amorphous-layer-inserted MANOS stack. 10nm AlSiOx (86%SiO2) was employed as an amorphous layer.

Fig. 11 Comparison of P/E window between MANOS and AlSiOx-inserted MANOS with 900°C PGA for 300s. There is no significant difference in P/E window between the two stacks.

Fig. 12 Comparison of retention at 125°C between MANOS and AlSiOx-inserted MANOS stacks with 900°C PGA for 300s. The superior retention was observed in AlSiOx-inserted MANOS. The initial storage charges, by programming were made with 1x1017/cm2 in the stacks.