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Roles of Traps Generated in Al_2O_3 Film with respect to Memory Characteristics in MANOS

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Introduction

Coupling interference from adjacent cells is one of the key issues in further scaling of floating-gate flash memories. Recently, charge-trap memories have been extensively studied in view of their immunity to the coupling interference. MANOS (Metal/Al_2O_3/SiN/SiO_2/Si) stacked structure is a commonly used charge-trap memory owing to its wide memory window and good retention characteristics [1, 2]. In this stack, it is generally believed that SiN provides trap sites and Al_2O_3 blocks charge transfer between SiN and gate electrode [1]. However, the stack without SiN layer also showed memory characteristics [3, 4]. By comparing memory characteristics of stacks with and without SiN trapping layer, we quantitatively confirmed for the first time that Al_2O_3 provides most of the traps. We also investigated effects of annealing on the trap characteristics of Al_2O_3 layer in detail. Moreover, we demonstrate a structure that simultaneously provides a sufficient amount of traps and good retention characteristics.

Experimental

Thin SiO_2 films (tunnel oxides) were thermally grown on n- and p-types of Si substrate. SiN and Al_2O_3 films were subsequently deposited by CVD on the SiO_2. In some of the samples (MAOS: Metal/Al_2O_3/SiO_2/Si sub.), SiN deposition was skipped [3]. TiN (10nm)/W (50nm) /TiN (10nm) of metal gate electrodes was formed. Several conditions of PGA (post-gate annealing) were applied in N_2 at 750°C~ 1000°C. MONOS (Metal/SiO_2/SiN/SiO_2/Si-sub.) stack was separately prepared as a reference. Block SiO_2 was formed by HTO-CVD in this stack. All of the samples were finished by forming gas annealing at 400°C for 30min. Sample structures, annealing conditions, and abbreviations of the sample names are summarized in **Table 1**.

C-V and I-V characteristics were measured for these capacitors before and after program (positive-biased) and erase (negative-biased) operations. The effect of light irradiation was also examined for n-substrate (pMOS) capacitor to confirm the effect of hole injection from substrate in negative-biased conditions.

Results and Discussion

Fig.1 shows dependence of program/erase (P/E) bias on V_{FB} shifts in MAOS and MANOS structures. Regardless of carrying out the PGA, almost the same amount of positive V_{FB} shift was observed in MAOS as in MANOS, even though MAOS does not have special charge-trap layers such as SiN. This result indicates Al_2O_3 layer provides most of the electron trap sites in two of these stacked structures [3, 4]. In the case of erase operation, negative V_{FB} shifts were observed both in MANOS and MAOS with PGA, whereas it was not observed without PGA. This is probably due to trapping of holes injected from substrate in hole trap sites generated in Al_2O_3 during PGA. **Fig.2** shows an effect of light irradiation on erase characteristics of MANOS stacked pMOS capacitor with PGA. Negative V_{FB} shift was observed only when erase operations were carried out with light irradiation, i.e. a sufficient number of holes were supplied from substrate. Positive V_{FB} shifts due to reverse tunneling from gate electrodes were not observed in either case. Thus, we conclude that the negative V_{FB} shifts under negative biased conditions are caused by trapping of holes injected from substrates. Then, to confirm where the hole trap sites were formed in the stacks, we compared the erase characteristics of MAOS, MANOS and MONOS for various PGA temperature. As shown in **Fig.3**, the negative V_{FB} shifts were observed when Al_2O_3 films were inserted in the stacks (MAOS and MANOS). On the other hand, no negative V_{FB} shifts were observed in MONOS. Moreover, negative V_{FB} shifts increased as the annealing temperature increased. These results strongly suggest that the hole trap sites were not generated in SiN and SiO_2, but generated in Al_2O_3 or at Al_2O_3/SiO_2 interface during PGA.

Changes of physical properties of Al_2O_3 by high-temperature annealing were also investigated. XRR, TEM and electron diffraction were carried out for various annealing conditions of Al_2O_3. As shown in **Fig.4**, density of Al_2O_3 was increased by annealing above 750°C. **Fig.5** shows plan-view TEM images and electron diffractions taken from these samples. Crystallization of Al_2O_3 is clearly observed in 1000°C 0.1s and 750°C 3600s annealed samples. Changes in density indicated in **Fig.4** are thought to be an effect of crystallization of Al_2O_3. **Fig.6** shows the relationship between negative V_{FB} shifts erased at Vg=-18V and density of Al_2O_3. The negative V_{FB} shift clearly increases as the Al_2O_3 density increases. This indicates that generation of hole trap sites is related to Al_2O_3 crystallization.

Degradation of retention was also observed in high-temperature annealed samples, as shown in **Fig.7**. This is thought to be another effect of generation of the trap sites. For further analysis of the effect of trap sites on the retention characteristics, we investigated the temperature dependence of leakage current (J_g). Strong temperature dependence on J_g was observed in the sample annealed at 900°C for 300s (**Fig.8(b)**), whereas only a slight dependence was observed in that annealed at 900°C for 0.1s (**Fig.8(a)**). **Fig. 9** shows activation energies (ΔE_a), extracted from temperature dependence by using the relationship of $\Delta E_a = -kT ln(J_g/J_g^0)$, assuming PF emission. Four levels of ΔE_a's (0.12eV, 0.18eV, 0.21eV, and 0.25eV) were extracted in the case of 300s PGA. These defects, which formed electron leakage paths, were located at energy levels of 0.12~0.25eV below the bottom of conduction band of Al_2O_3. It should be noted that these defects closely related to the traps are essential for the memory characteristics themselves. In fact, there are some trade-off relationships between memory windows and retention characteristics as shown in **Figures 6** and **7**.

Finally we demonstrated a method for suppressing degradation of retention on the basis of the above understanding. An amorphous layer was inserted between Al_2O_3 and metal gate, as shown in **Fig.10**. It simultaneously enables elimination of leakage paths through blocking oxide and keeping of almost the same amount of electron or hole traps. A 10nm-thick Si-rich $AlSiO_x$ was deposited as the amorphous layer. **Fig.11** shows comparison of P/E window between MANOS and $AlSiO_x$-inserted MANOS. There are no significant differences between the two stacks. **Fig.12** shows a comparison of retention between MANOS and $AlSiO_x$-inserted MANOS. As expected, $AlSiO_x$-inserted MANOS shows excellent retention characteristics.

Conclusion

We have systematically investigated the impact of annealing process on generation of traps and defects in Al_2O_3 films, and revealed that traps and defects in Al_2O_3 induced by thermal process play an important role in realizing the memory characteristics of MANOS. Furthermore, we have demonstrated the improvement of retention by $AlSiO_x$-inserted MANOS.

Reference

[1]C. H. Lee, et al., Ext. abstract of SSDM2002, 162
[2]C. H. Lee, et al., IEDM Tech. Dig. 2003, 613
[3]M. Specht, et al., Solid-State Electron, 49,716(2005)
[4]A. Kerber, et al., J. Appl. Phys., 94, 6627(2003)

Table 1 Fabricated stack structures in this work

	MAOS	MANOS	MONOS
Metal	TiN/W/TiN	TiN/W/TiN	TiN/W/TiN
Block Ox	20nm-Al_2O_3	20nm-Al_2O_3	10nm HTO
Charge trap	-	10nm-SiN	10nm-SiN
Tunnel Ox	6nm-SiO_2	3.5nm-SiO_2	3.5nm-SiO_2
Si sub	p-type	n-, p-type	p-type
Post gate Annealing (PGA) in LP-N_2			
temperature	750~1000°C		
time	0.1~3600s		

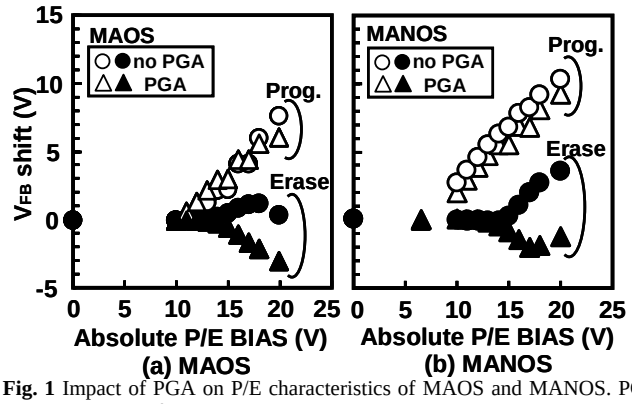

Fig. 1 Impact of PGA on P/E characteristics of MAOS and MANOS. PGA was performed at 900°C for 0.1s. Pulse times of program/erase are 50ms/pulse × 200times. V_{FB} shifts are difference between V_{FB} at fresh and V_{FB} after P/E.

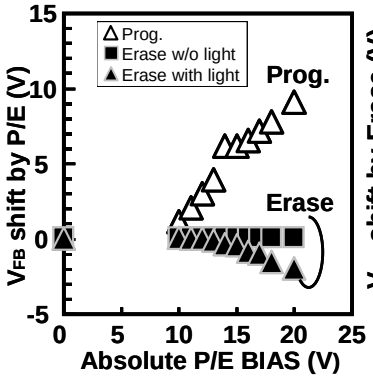

Fig.2 Comparison of erase behavior between light irradiation and no irradiation in MANOS stacked pMOS capacitor with PGA at 900°C for 0.1s. P/E operation performed for 50ms/pulse × 200times at each bias condition.

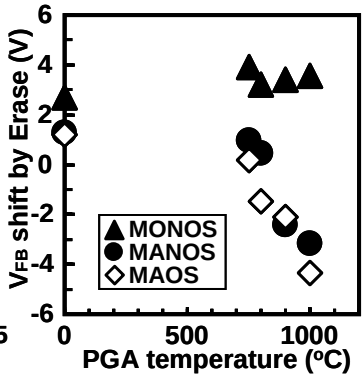

Fig.3 Negative V_{FB} shift by erasing dependence of PGA temperature in MANOS, MAOS and MONOS stacks. Erase operation was performed at -18V for 50ms/pulse × 200 times.

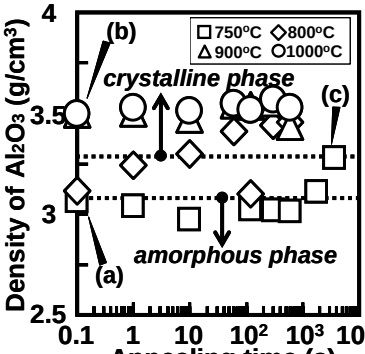

Fig.4 Al_2O_3 density dependence of annealing at 750°C~1000°C with various times for 20nm-Al_2O_3/ 6nm-SiO_2 stack. Al_2O_3 densities were obtained from XRR analysis.

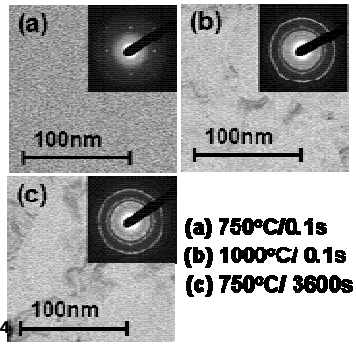

Fig.5 Plan-view TEM images and electron diffraction patterns of Al_2O_3 films with PGA at (a) 750°C for 0.1s, (b)1000°C for 0.1s and (c)750°C for 3600s, corresponding to point (a) ~ (c) in **Fig.4**.

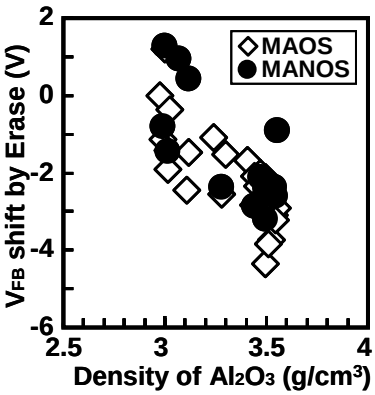

Fig.6 Relationships between negative V_{FB} shift by erased at -18V and density of annealed Al_2O_3 with various conditions in MAOS and MANOS. Annealing in the range of 750~1000°C was performed for 0.1~ 3600s.

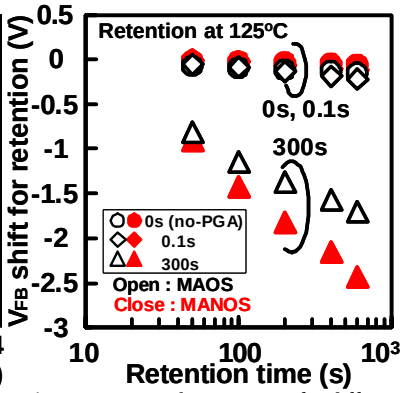

Fig. 7 Retention characteristics for different annealing times at 900°C PGA with MAOS and MANOS stack, showing the degradation of retention with PGA time increase. The initial storage charges by programming were made with 1x10^{13}/cm^2 in the stacks.

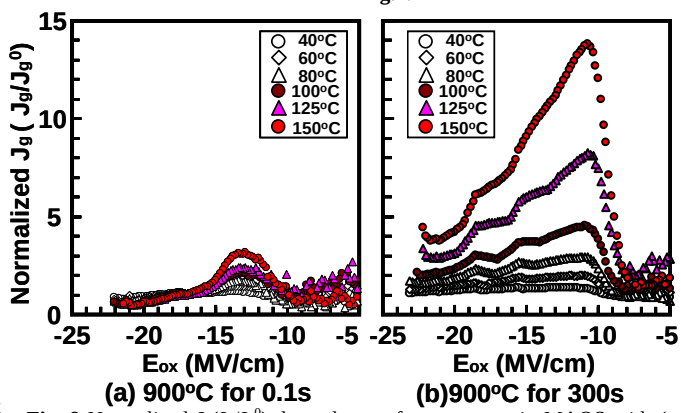

Fig. 8 Normalized $J_g(J_g/J_g^0)$ dependence of temperature in MAOS with (a) PGA at 900°C for 0.1s and (b) PGA at 900°C for 300s as a function of applied electrical field (E_{ox}). J_g were normalized by dividing by J_g at 25°C (J_g^0).

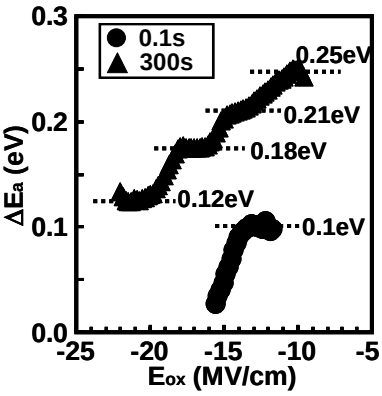

Fig. 9 Comparison of ΔE_a between 0.1s and 300s annealing at 900°C. ΔE_a's were obtained from Fig.8 by using the relationship of ΔE_a=-kT*ln*(J_g/J_g^0), assuming PF emission.

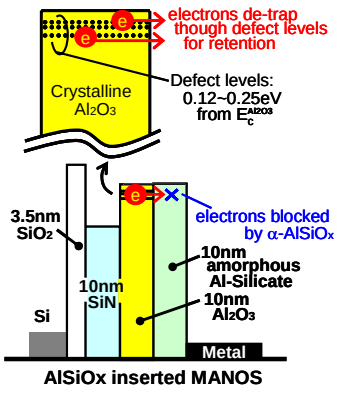

Fig.10 Schematic illustration of amorphous-layer-inserted MANOS stack. 10nm $AlSiO_x$ (86%SiO_2) was employed as an amorphous layer.

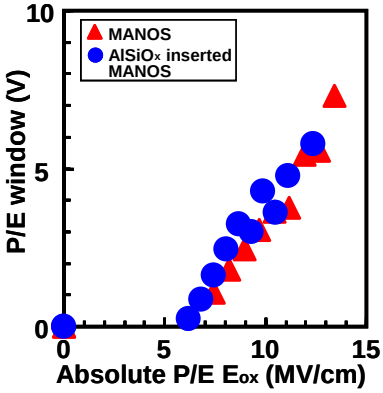

Fig.11 Comparison of P/E window between MANOS and $AlSiO_x$-inserted MANOS with 900°C PGA for 300s. There is no significant difference in P/E window between the two stacks.

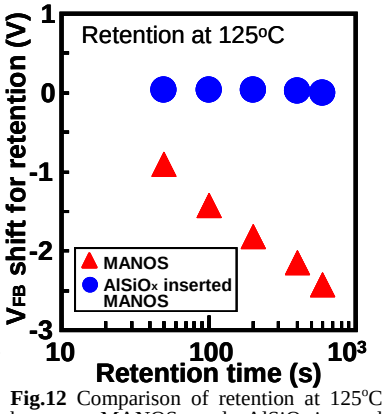

Fig.12 Comparison of retention at 125°C between MANOS and $AlSiO_x$-inserted MANOS stacks with 900°C PGA for 300s. The superior retention was observed in $AlSiO_x$ inserted MANOS. The initial storage charges by programming were made with 1x10^{13}/cm^2 in the stacks.