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SONOS-Type Nonvolatile Memory Formed on Epitaxial-Ge Layer on Si Substrate

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1. Introduction

Ge-based MOS devices have exhibited the great potential to drive next-generation ULSI technology [1-2]. If incumbent nonvolatile memory can be successfully integrated on a Ge layer instead of a conventional Si substrate, the memory device with even more superior performance is highly expected in the following aspects. The data access speed can be significantly improved because of the enhanced current drive due to the intrinsically higher carrier mobility. For program operation driven by channel hot electron injection, Ge source/drain would facilitate the efficiency of primary impact ionization and consequently increase the program speed due to the smaller bandgap (E_g) compared with the Si counterpart. For the same reason, secondary impact ionization rate will also be boosted which is very helpful to activate the mechanism of channel initiated secondary electron (CHISEL) [3] and therefore the program speed can be accelerated. The smaller bandgap for Ge also shows the advantage in improving the program speed for p-channel memory devices operated by band-to-band tunneling induced hot electron (BBHE) due to the increased generation rate of the electron/hole pair from band-to-band tunneling. In fact, this concept has been verified by replacing a Si channel with a SiGe one in a nonvolatile memory [4]. On the other hand, the erase speed for those operated by band-to-band tunneling induced hot hole (BBHH) is also enhanced due to the bandgap nature of Ge. Nevertheless the augmented performance will be obtained; nonvolatile memory devices formed on Ge have never been reported which may be primarily due to the lack of an appropriate tunnel dielectric for Ge passivation along with the costly Ge substrate. To overcome these limitations, we have successfully developed a process to form an epitaxial Ge layer topped by thermal SiO_2 with good interface properties on a Si substrate and the eligibility of this structure for device operation has been evidenced by the high-performance Ge MOSFET [1-2]. Based on our previous research results, SONOS-type nonvolatile memory devices formed on the Ge layer were investigated in this work as the pioneering research for the future Ge-based memory technology.

2. Experiment

P-type Si substrates were used as the starting material to fabricate SONOS-type nonvolatile memory devices on the Ge layer. A $Si_{0.3}Ge_{0.7}$ layer was first formed in the pre-defined active area by the deposition of thin amorphous Ge and a subsequent annealing. Then oxidation of the $Si_{0.3}Ge_{0.7}$ layer followed by a forming gas annealing was performed to form the epitaxial Ge layer topped by thermal SiO_2 on a Si substrate. After an etching-back process by dilute HF solution, the thermal SiO_2 was thinned down to be 10.1 nm and was employed as the tunnel dielectric. The detailed process condition was disclosed in our previous publication [5]. Next, 14.0-nm nitrogen-rich Si_3N_4 film with refractive index of 1.988 was deposited in a LPCVD furnace as the charge trapping layer. Then the blocking oxide was formed by 13.0 nm-SiO_2 deposition in a PECVD chamber using tetraethoxysilane (TEOS) as the precursor. Finally aluminum was deposited and patterned as the gate electrode. Since the tunnel dielectric quality is the major concern for the Ge-based memory, the samples without Si_3N_4 film deposition were also prepared to verify whether the charges are stored in the tunnel dielectric or in the Si_3N_4 film. Note that although the advantages of the Ge-based memory should be verified by transistor-type devices, to achieve the desirable Ge-based memory, the basic memory effect and the tunnel dielectric should be first qualified and therefore capacitor-type devices were employed in this work to assess the electrical characteristics.

3. Results and Discussion

Fig. 1 is the capacitance-voltage (C-V) hysteresis after bidirectional voltage sweepings for the Ge-based memory. As shown in the inset of Fig. 1, with the range of sweeping voltage increases from ±8, ±12 and ±16 V, the hysteresis memory window changes from 1.8, 8.3 and 15.3 V respectively. For the inset, it shows that the sample without Si_3N_4 film presents a negligible memory window which confirms that the amount of traps in the tunnel dielectric is small and the charges are indeed stored in the Si_3N_4 film. The program and erase transient characteristics for the Ge-based memory operated by Fowler–Nordheim (FN) mechanism are shown in Fig. 2 to assess its operation speed. The high operation speed is evidenced by flatband voltage (V_{FB}) shift of 4.2 V with -16 V erase voltage for 1 ms which is superior to the Si-based SONOS memory [6] using similar nitrogen-rich Si_3N_4 as the charge trapping layer. However, there exists the asymmetry in program and erase speed. This phenomenon may be due to the thin $SiGeO_x$ layer at the tunnel dielectric/Ge layer interface which is caused by the incomplete reduction process during the forming gas annealing and it would result in an asymmetric band structure during program and erase operation as revealed in Fig. 3. It is clear that the tunnel dielectric is actually composed of the thin $SiGeO_x$ and the bulk SiO_2. Since the bandgap and dielectric constant (ε) of the $SiGeO_x$ is between GeO_2 (E_g: 5.7 eV, ε:~7) and SiO_2 (E_g: 9 eV, ε: 3.9), the tunnel dielectric has the structure similar to that of VARIOT dielectric [7]. For this VARIOT-like tunnel dielectric, if elec-

trons are tunneling from the Si_3N_4 film, they experience a thinner barrier because the electric field redistributes in the two layers due to Gauss' law as shown in the left of Fig. 3 which corresponds to erase operation and consequently makes a higher speed. On the other hand, for program operation, electrons are tunneling from the Ge layer and experience two barriers as shown in the right of Fig. 3 which makes the tunneling more difficult and therefore a slower speed. The retention characteristics at room temperature and 125 °C for the Ge-based memory are displayed in Fig. 4. About 15 % and 21 % charge loss after 10-year operation at room temperature and 125 °C was respectively observed. The inset of Fig. 4 represents the data endurance measured by programming at +16 V for 10 ms and erasing at -16 V for 1 ms. A negligible degradation of the memory window was observed up to 10^4 program/erase cycles which implies the satisfactory reliability characteristics.

4. Conclusion

With Si substrates, SONOS-type nonvolatile memory devices with the SiO_2-tunnel dielectric were fabricated on a Ge layer in this work. This Ge-based memory has demonstrated a large hysteresis memory window, a high erase speed, a good retention along with robust data endurance, which qualify the SiO_2 on Ge as the eligible tunnel dielectric. Most importantly, the process can be fully integrated with incumbent ULSI technology and paves the way for the fulfillment of next-generation nonvolatile memory.

Acknowledgments

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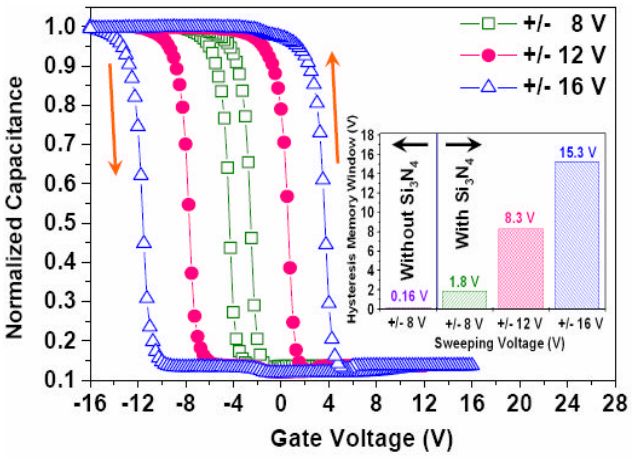

Fig. 1 C-V hysteresis for the Ge-based memory. The inset is the hysteresis memory window for different ranges of sweeping voltage and the memory window for the sample without Si_3N_4 is also shown for comparison.

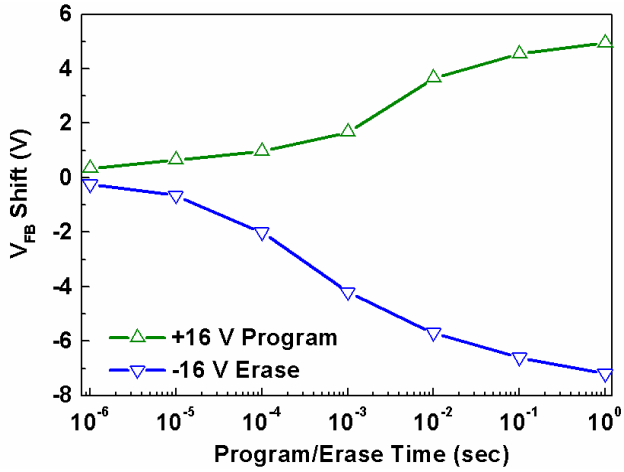

Fig. 2 P/E transient characteristics for the Ge-based memory.

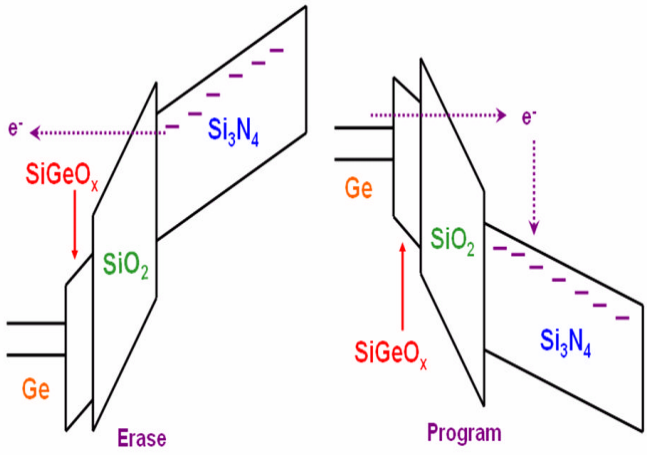

Fig. 3 Energy band diagram schematics for program and erase operation.

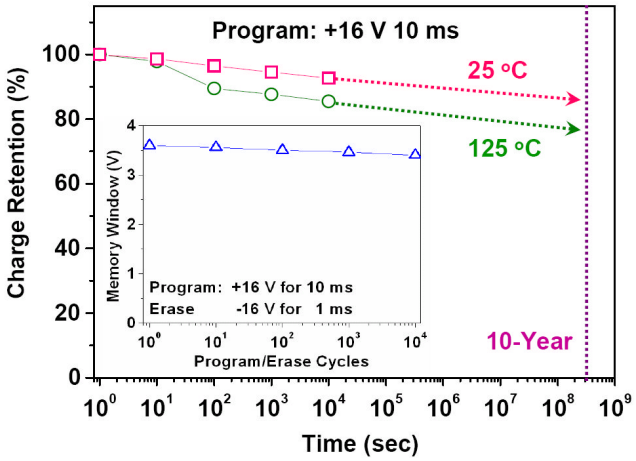

Fig. 4 Retention characteristics at room temperature and 125 °C for the Ge-based memory. The inset displays the data endurance performance for the Ge-based memory.