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A 1.2V Operation 2.43 Times Higher Power Efficiency Adaptive Charge Pump Circuit with Optimized V_{TH} at Each Pump Stage for Ferroelectric (Fe)-NAND Flash Memories

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1. Introduction

The Ferroelectric (Fe)-NAND flash memory device [1-3] and high-speed highly reliable memory circuits [4] were proposed to decrease the power consumption of data centers (Fig.1,2). Key benefits of Fe-NAND are 1) a high reliability where the program/erase cycles increases from 10^4 to 10^8 cycles and 2) a low voltage/power consumption where the program/erase voltage decreases from 20V of the floating-gate NAND to 6V. As the feature size decreases below 30nm, the inter bit-line capacitance drastically increases and the power consumption increases by 38% [5]. By decreasing the power supply, V_{DD}, from 3.3V to 1.2V, the power consumption of the memory core decreases by 87%. However, the power consumption of the conventional charge pump [6] to generate read/program/erase voltage triples [7]. To realize low voltage and low power Fe-NAND flash memories, this paper proposes an adaptive charge pump that increases the power efficiency and the output voltage by 143% and 25% without circuit area and process step penalty.

2. Problems of the Conventional Charge Pump

In the proposed 1.2V Fe-NAND flash memory, V_{READ} and V_{PGM} charge pump circuits generate a read voltage, 2V and a program voltage, 6V from V_{DD}, 1.2V (Fig.1). Fig.3(a)(b) shows the conventional charge pump. The transistor V_{TH} of all pump stages is fixed at V_{TH_MOS}. As shown in Fig.4(a),(b), V_{TH_MOS} has optimal values to maximize the power efficiency or the output voltage, V_{OUT}. If V_{TH_MOS} is too high, the large V_{TH} loss of MOS diodes decreases the power efficiency and V_{OUT}. On the other hand, if V_{TH_MOS} is too low, the transistor does not function as a rectifier and the output current flows backward from the output to the input. The optimal V_{TH_MOS} of the conventional V_{PGM} charge pump to maximize the power efficiency is -0.6V (Fig.4(b)) that is lower than the conventional V_{READ} charge pump, -0.3V (Fig.4(a)). In the V_{PGM} charge pump as V_{OUT} is higher than that of the V_{READ} charge pump, the V_{TH} increases due to the larger body effect and thus the optimal V_{TH_MOS} becomes lower. If V_{TH_MOS} is -0.3V to maximize the power efficiency of the V_{READ} charge pump, the power efficiency of the V_{PGM} charge pump is 127% smaller than the optimal value with V_{TH_MOS}=-0.6V. Similarly, if V_{TH_MOS} is -0.5V to maximize V_{OUT} of the V_{READ} charge pump, V_{OUT} of the V_{PGM} charge pump decreases by 19% from its maximum value with V_{TH_MOS}=-1.0V.

3. Proposed Dual V_{TH} Charge Pump Circuit

To increase the power efficiency and V_{OUT} of the V_{PGM} charge pump, this paper proposes a dual V_{TH} charge pump (Fig.3(c)(d)). Ferroelectric (Fe)-FETs are used as diodes to change the V_{TH} by the program/erase. There is no area or process overhead as Fe-FETs in the charge pump are fabricated with the same process steps as memory cells. The V_{TH} of V_{READ} and V_{PGM} charge pumps are uniform with V_{TH_READ} and V_{TH_PGM}. By changing the V_{TH} of Fe-FETs, V_{TH_READ} and V_{TH_PGM} are independently optimized at -0.3V (Fig.4(a)) and -0.6V (Fig.4(c)). As a result, the power efficiency of the V_{PGM} charge pump increases by 127%. By selecting V_{TH_READ} and V_{TH_PGM} as -0.5V and -1.0V, V_{OUT} of both V_{READ} and V_{PGM} charge pumps are also maximized. V_{OUT} of the V_{PGM} charge pump increases by 19%.

4. Proposed Adaptive Charge Pump Circuit

To further increase the power efficiency and V_{OUT}, this paper also proposes an adaptive charge pump (Fig.3(e)(f)). The V_{TH} of both V_{READ} and V_{PGM} charge pumps are different with $V_{TH\_Fe1,\,2...8}$ at each pump stage. $V_{TH\_Fe1,\,2...8}$ has a relationship of $V_{TH\_Fe1} > V_{TH\_Fe2} > \ldots > V_{TH\_Fe8}$ because at a pump stage closer to the output the source voltage increases and the V_{TH} shift due to the body effect also increases. Fig.5 shows the simulated power efficiency and V_{OUT} of the adaptive charge pump. Compared with the dual V_{TH} charge pump, the adaptive charge pump increases the power efficiency and V_{OUT} by 6.9% and 4.5%. Table 1 summarizes the conventional and proposed charge pumps. The adaptive charge pump is most power efficient and has the highest V_{OUT} as the V_{TH} at each pump stage is best optimized. Compared with the conventional charge pump, the power efficiency and V_{OUT} increase by 143% and 25%.

5. Measurement Results

Fig.6 shows the detailed operation of the proposed adaptive charge pump. Fig.6(a) shows the boosting to generate V_{READ}, 2V and V_{PGM}, 6V from V_{DD}. During the boosting, the well of Fe-FETs is grounded so that the V_{TH} of Fe-FETs is fixed at the optimal values. Erase, program and the V_{TH} measurement (Fig.6(b),(c),(d)) are performed only once during the testing to adjust the V_{TH}. A high voltage such as program/erase voltage biased to Fe-FETs inputs from the testing equipment. As the first step of the V_{TH} adjustment, the erase is performed by biasing the well of Fe-FET to 6V (Fig.6(b)). $V_{TH\_Fe1,\,2...8}$ all increases to a positive value. Next, the program voltage, 5~6V, is applied to the gate of Fe-FETs and $V_{TH\_Fe1,\,2...8}$ decreases (Fig.6(c)). In the V_{TH} measurement, a negative V_{TH} is measured by applying 1V to the source, 1.1V to the drain and 0~1V to the gate (Fig.6(d)). Program and the V_{TH} measurement are repeated until the V_{TH} at each pump stage reaches the optimal value.

Fig.7 shows a microphotograph of the proposed circuit. Fig.8 shows measured V_{OUT} versus the V_{TH}. As the V_{TH} decreases, V_{OUT} increases, which is consistent with simulated results. Fig.9 (a) shows the measured V_{TH} shift of Fe-FETs due to the disturb during the boosting. Fig.9 (b) describes the disturb of Fe-FETs. While a voltage higher than V_{DD} is biased to Fe-FETs, the V_{TH} shift of Fe-FET is negligibly small irrespective of the operation cycles and V_{DD} and a highly reliable operation is realized.

6. Conclusion

A 1.2V adaptive charge pump for low power Fe-NAND is proposed and experimentally demonstrated. The chip is fabricated with the CMOS compatible Fe-FET process [1]. By using Fe-FETs as diodes in the charge pump and optimizing the V_{TH} at each pump stage, the power efficiency and V_{OUT} increase by 143% and 25% without circuit area and process step penalty. Fe-FETs in the proposed circuit are immune to the disturb and a highly reliable operation is experimentally demonstrated.

Acknowledgements

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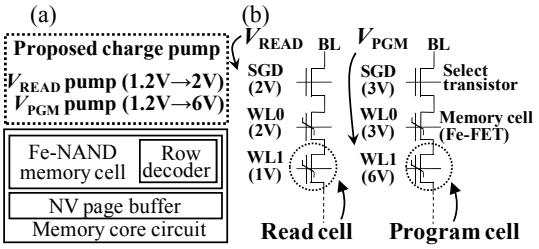

Fig.1 (a) Circuit diagram of the Fe-NAND flash memory. (b) Read and program of Fe-NAND.

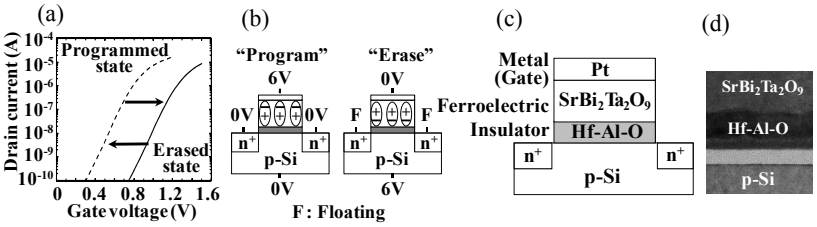

Fig.2 (a) I_D-V_G characteristics after the program and erase. (b) Program and erase bias condition. (c) Fe-NAND cell structure. (d) SEM photograph.

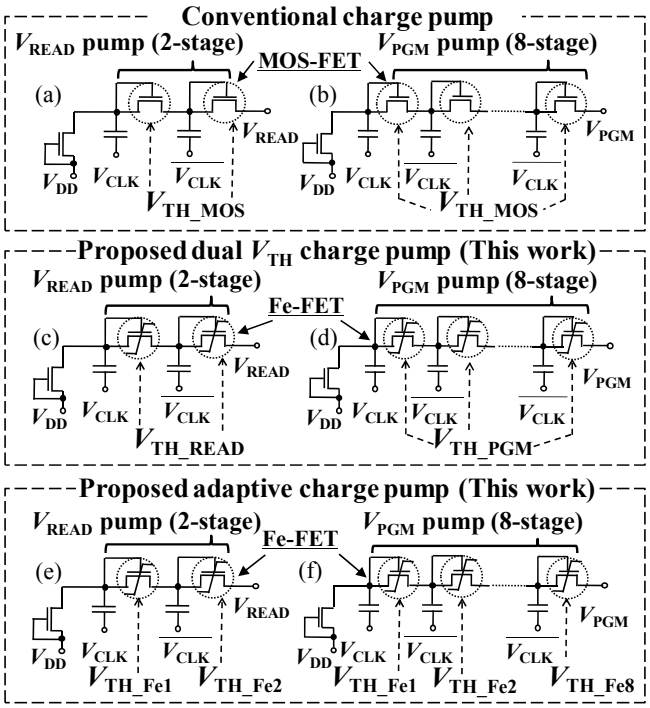

Fig.3 Charge pump circuits. (a),(b) Conventional V_{READ} and V_{PGM} charge pump. The V_{TH} are fixed at V_{TH_MOS}. (c),(d) Proposed dual V_{TH} charge pump. The V_{TH} of V_{READ} and V_{PGM} charge pumps are uniform with V_{TH_READ} and V_{TH_PGM}. V_{TH_READ} and V_{TH_PGM} are independently optimized. (e),(f) Proposed adaptive charge pump. The V_{TH} of each transistor in V_{READ} and V_{PGM} charge pumps are different with $V_{TH\_FE1,2...8}$ and are best optimized to maximize the power efficiency of both V_{READ} and V_{PGM} charge pumps.

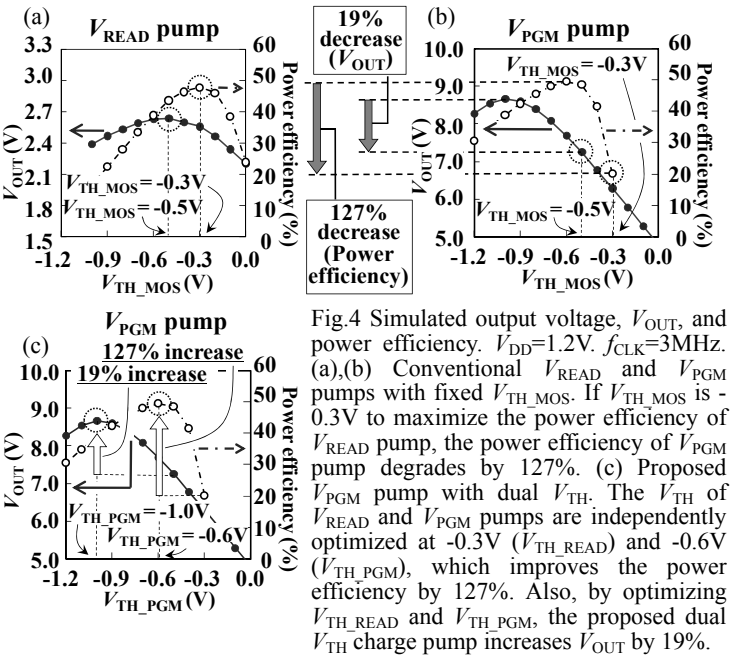

Fig.4 Simulated output voltage, V_{OUT}, and power efficiency. V_{DD}=1.2V. f_{CLK}=3MHz. (a),(b) Conventional V_{READ} and V_{PGM} pumps with fixed V_{TH_MOS}. If V_{TH_MOS} is -0.3V to maximize the power efficiency of V_{READ} pump, the power efficiency of V_{PGM} pump degrades by 127%. (c) Proposed V_{PGM} pump with dual V_{TH}. The V_{TH} of V_{READ} and V_{PGM} pumps are independently optimized at -0.3V (V_{TH_READ}) and -0.6V (V_{TH_PGM}), which improves the power efficiency by 127%. Also, by optimizing V_{TH_READ} and V_{TH_PGM}, the proposed dual V_{TH} charge pump increases V_{OUT} by 19%.

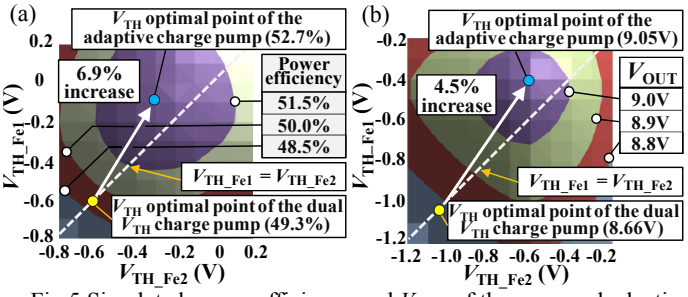

Fig.5 Simulated power efficiency and V_{OUT} of the proposed adaptive charge pump. The V_{TH} of each transistor is individually optimized. (a),(b) Power efficiency and V_{OUT} of V_{PGM} pump vs. V_{TH_Fe1} and V_{TH_Fe2}. Compared with the proposed dual V_{TH} charge pump, the power efficiency and V_{OUT} increase by 6.9% and 4.5%.

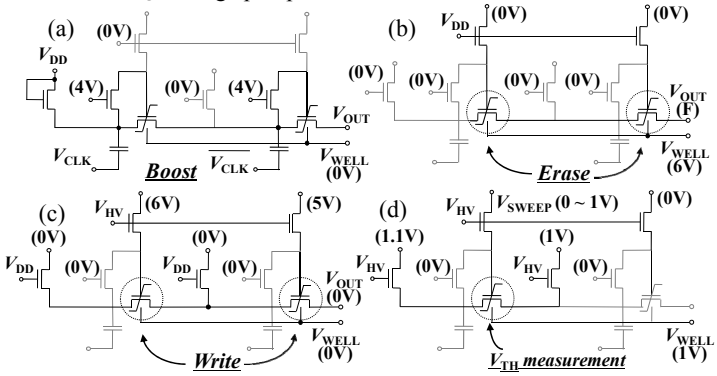

Fig.6 Operation principle of the proposed adaptive charge pump. (a) Boost. (b) Erase. (c) Program. (d) V_{TH} measurement. (b),(c),(d) are performed only once during the testing to adjust the V_{TH}. High voltage such as write/erase voltage input from the testing equipment.

Table 1 Comparison of the conventional and the proposed charge pump circuits. V_{OUT} is the output voltage.

	Conventional charge pump	Proposed dual V_{TH} charge pump	Proposed adaptive charge pump
Power efficiency (%)	21.7 (x1.00)	49.3 (x2.27)	52.7 (x2.43)
V_{OUT} (V)	7.26 (x1.00)	8.66 (x1.19)	9.05 (x1.25)
Circuit area (a.u.)	1	1	1

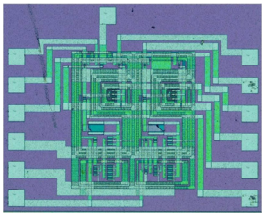

Fig.7 Chip microphotograph of the proposed adaptive V_{READ} pump.

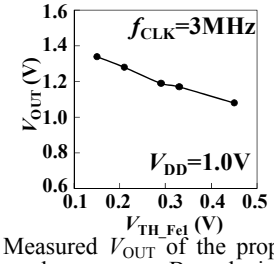

Fig.8 Measured V_{OUT} of the proposed adaptive charge pump. By reducing the V_{TH}, V_{OUT} increases.

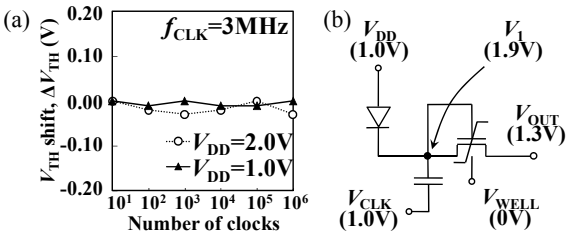

Fig.9 (a) Measured V_{TH} shift of Fe-FETs caused by the disturb during the boosting. (b) Bias condition of the disturb. Since the measured V_{TH} shift is negligibly small irrespective of the operation cycles and the power supply, V_{DD}, the proposed circuit is immune to the disturb.