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Direct Measurement of Back-Tunneling Current during Program/Erase Operation of MONOS Memories and Its Dependence on Gate Work Function

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Introduction

MONOS memory is one of the candidates to replace floating gate (FG) non-volatile memory with its simple structure and less cell-to-cell interference [1]. Although multi-level cell operation is expected in MONOS memories to realize high density data storage, leakage current and back-tunneling current during program/erase (P/E) operation bring about Vth saturation [2] and narrow Vth window. Besides, it is known that penetration current severely degrades device reliability [3]. Thus, it is necessary to analyze current components of MONOS devices. Based on the charge-centroid extraction method [4][5], we have developed an analysis method which enables extracting back tunneling current component. In this paper, gate work function dependence of back-tunneling current during P/E operation is discussed to confirm the validity of our analysis scheme.

Analysis Method

The electrical distance of charge centroid (z_{eff}) from a gate electrode is derived as [4][5]:

$$z_{eff} = -\varepsilon_{ox}\Delta V_{fb} / Q_{trap} \quad (1)$$

where Q_{trap} is the charge trapped in the nitride layer, ε_{ox} is dielectric constant of SiO_2 and ΔV_{fb} is the flat-band voltage shift during P/E operation. To eliminate an error due to penetration current, z_{eff} is defined as a fixed value ($z_{eff.fix}$) once it is derived from a short time domain in P/E operation, thereby assuming 100% carrier capture efficiency. Q_{trap} is then derived in all time range as:

$$Q_{trap} = -\varepsilon_{ox}\Delta V_{fb} / z_{eff.fix} \ . \quad (2)$$

Now, measured injected charge Q_{inj} [5] is the sum of trapped charges Q_{trap} and leakage/back-tunneling charges Q=Q_{leak}+ Q_{back}, as shown in Fig.1:

$$Q_{inj} = Q_{trap} + Q = Q_{trap} + Q_{leak} + Q_{back} \quad (3)$$

where Q_{leak} is the injected charge from a Si-substrate that is not captured in the nitride layer. As time derivative of equation (3), current components are expressed as:

$$J_{inj} = J_{trap} + J = J_{trap} + J_{leak} + J_{back} \ . \quad (4)$$

If the back-tunneling current (J_{back}) is comparable or larger than the other current components, J_{back} can be distinguished by observing the dependence on the electric fields of the tunnel oxide (E_{OX}) and the block oxide (E_{BLK}),

$$E_{OX} = \left(V_G - V_{fb} - \phi_S\right) / \left(T_{OX} + T_{SiN} + T_{BLK}\right) \quad (5)$$

$$E_{BLK} = \left\{V_G - E_{ox}(T_{ox} + T_{SiN}) - \phi_S - \psi_{ms}\right\} / T_{BLK} \quad (6)$$

where V_G is gate voltage, T_{ox}, T_{SiN}, T_{BLK} are electrical thicknesses as depicted in Fig.1. ϕ_s and ψ_{ms} are silicon band bending and the work function difference between silicon substrate and gate electrode, respectively. The principal of this distinction method is that J_{leak} is a unique function of E_{OX}, whereas J_{back} is uniquely dependent on E_{BLK}.

Experimental

The MONOS devices used in this paper are summarized in Table 1. The gate stack consists of 4-nm tunnel oxide, 5-nm SiN charge trap layer, and Al_2O_3 block dielectric. Cap SiN layer is deposited on top of the block oxide when using n^+poly-Si gate to suppress reaction between poly-Si and Al_2O_3. Metal gates are deposited by evaporation through a shadow mask. The area of the capacitors is 1×10^{-4} cm^2.

Back Tunneling from Polysilicon Gate during Erase Operation

Fig.2 shows V_{fb} shift as a function of time during erase operation of MONOS with n^+poly-Si gate. Charge centroid ($z_{eff.fix}$) extracted from a short time domain is located at around the SiN/Al_2O_3 interface, as depicted in the inset of Fig.2. Time evolutions of J_{inj} and J_{trap} are visualized in Fig.3. With increasing gate voltage, J_{inj} is boosted up and the trap efficiency (J_{trap}/J_{inj}) drops down deeper. The presence of back-tunneling current from the gate is evidenced when J_{inj} is plotted as a function of E_{BLK}. As shown in Fig.4, J_{inj} appears as a unique and increasing function of E_{BLK}. Hence we conclude that in MONOS devices with n^+poly-Si gate, J_{inj} mainly consists of J_{back} during deep erase operation.

Metal Work-Function Dependence of Back Tunneling

1) Erase Operation

The dependence of back-tunneling current on the work function of metal gate electrodes (Al, Mo, Au and Pt) during erase operation is summarized in Figs.5 and 6. In this comparison, erase voltage and initial V_{fb} are set to the same value for all metal electrodes. Time evolutions of J_{inj} and J_{trap} in Fig.5 indicate the increase of J_{inj} with a decrease of gate work function when entering into deep erase condition.

Fig.6 (a)-(d) shows J_{inj} and J_{trap} as a function of tunnel oxide electric field (E_{OX}) in a wide range of gate voltage (-12 ~ -18V). It is found that J_{trap}'s at different erase voltages form a common envelope curve corresponding to 100% carrier capture. It is also shown that J_{inj} at a low erase voltage (-12V) follow the envelope curve in all the metal gate materials. However, in Al gate, deviation of J_{inj} from the common curve is observed at higher erase voltages. The deviation of J_{inj} is only slightly observed for the highest erase voltage (-18V) in Mo gate. On the contrary, for the metal gates with even higher work function (Au and Pt), the deviation of J_{inj} is not observed at any erase voltage. The results indicate strong dependence of back tunneling current on the gate work function during deep erase operation.

2) Program Operation

Fig.7 shows J_{inj} as a function of time during program operation. Time evolution of J_{inj} is almost the same for all the gate materials, implying the absence of back tunneling current. This inference is confirmed by Fig. 8 (J_{inj} vs. E_{OX}), showing no deviation of J_{inj} from a common envelope curve even for the gate electrode with a high work function (Pt). Hence it is concluded that back-tunneling current from the gate is negligible during deep program operation.

3) Comparison of J_{inj} and J_{trap}

The summary of currents during program/erase operation is depicted in Fig.9. Injected current J_{inj} is a increasing function of gate voltage. Strong dependence of J_{inj} on gate work function is obtained during erase operation. On the contrary there is negligible dependence of J_{trap} on gate work function.

Conclusions

In this work, we proposed a new analysis scheme to distinguish back-tunneling current from measured injected current on MONOS devices. It is found that in deep program/erase condition, leakage or back-tunneling current is the dominant component of J_{inj}, respectively. Especially, J_{back} boosting is remarkable when using a gate electrode with low work function. In contrast, the dependence of J_{trap} on gate work function is found to be negligible. These results

give new information that is never obtained from analyzing J_{trap} (or V_{fb}-t) characteristics only. They will provide useful insight into reliability prediction of MONOS memories.

Acknowledgement

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References

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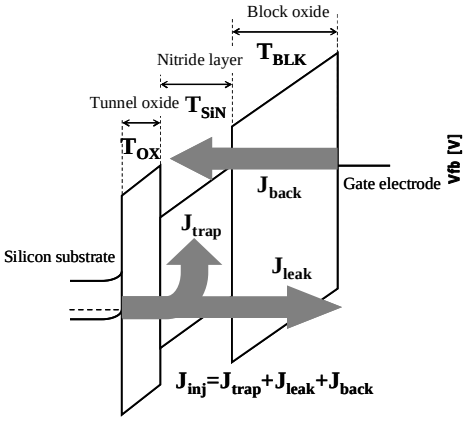

Fig.1 Current flow from Si-substrate (J_{trap}, J_{leak}) and back-tunneling current from gate electrode (J_{back}) during erase operation.

Table 1 MONOS samples used in this paper.

#	substrate	Tunnel oxide	Charge layer	Block oxide	Electrode
1	P	SiO2 4nm	SiN 5nm	Al2O3 17nm/Cap SiN 2nm	n+poly Si
2	P	SiO2 4nm	SiN 5nm	Al2O3 10nm	Al
3	P	SiO2 4nm	SiN 5nm	Al2O3 10nm	Mo
4	P	SiO2 4nm	SiN 5nm	Al2O3 10nm	Au
5	P	SiO2 4nm	SiN 5nm	Al2O3 10nm	Pt
6	N	SiO2 4nm	SiN 5nm	Al2O3 10nm	Al
7	N	SiO2 4nm	SiN 5nm	Al2O3 10nm	Mo
8	N	SiO2 4nm	SiN 5nm	Al2O3 10nm	Au
9	N	SiO2 4nm	SiN 5nm	Al2O3 10nm	Pt

Work function (eV) : Al(4.28), Mo(4.6), Au(5.1), Pt(5.65) from Herbert B. Michaelson, JAP **48**, 4729 (1977).

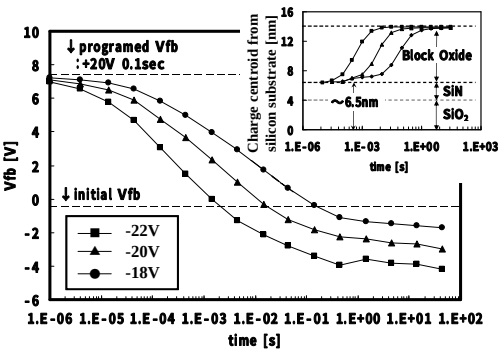

Fig.2 Erase characteristics of MONOS device with n^+poly silicon gate. The charge centroid is located around the SiN/Al_2O_3 interface (inset).

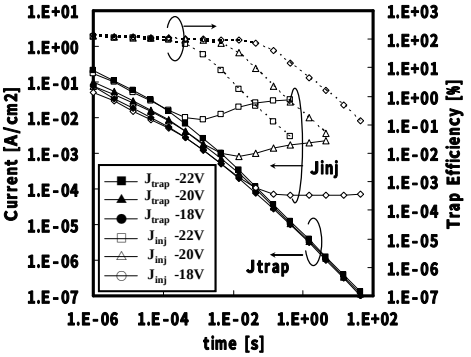

Fig.3 J_{trap} and J_{inj} extracted from erase operation of sample #1. J_{inj} boosting suggests back-tunneling current from gate electrode.

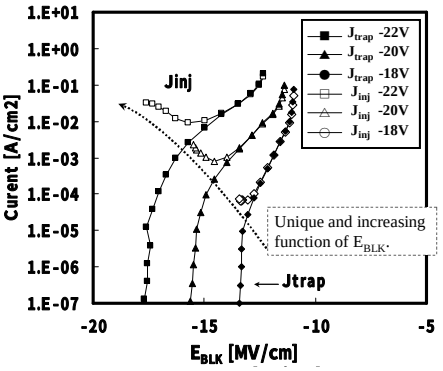

Fig.4 J_{inj} as a function of electric field of block oxide. J_{back} boosting is observed.

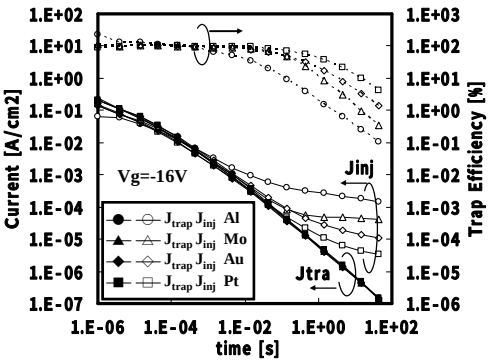

Fig.5 Work function dependence of J_{inj} during erase operation.

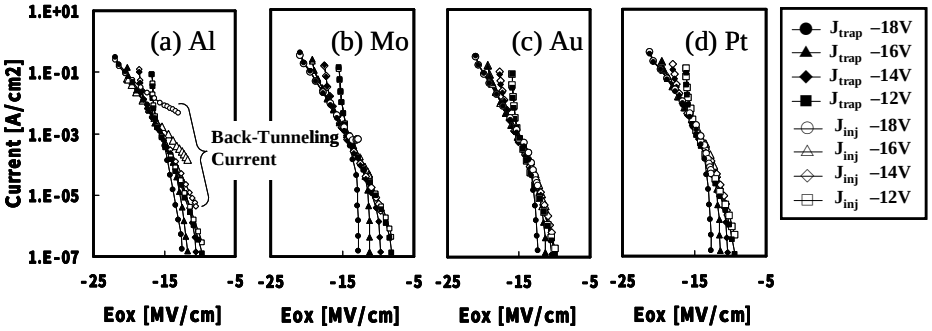

Fig.6 J_{inj} as a function of tunnel oxide electric field during erase operation with (a)Al gate, (b)Mo gate, (c)Au gate and (d)Pt gate. J_{back} boosting is observed when using Al gate.

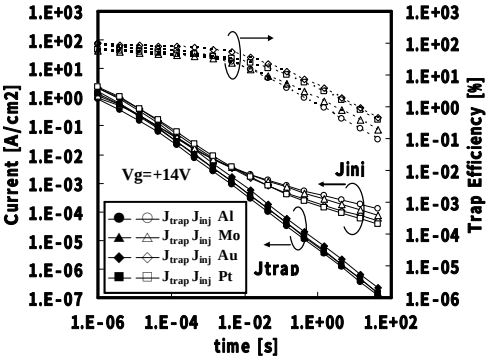

Fig.7 Work function dependence of J_{inj} during program operation.

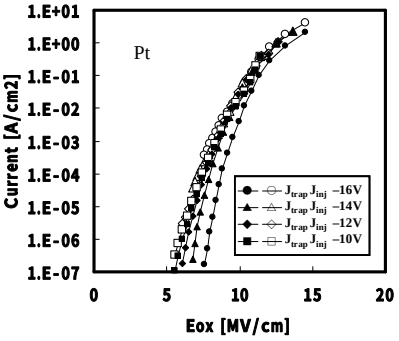

Fig.8 J_{inj} as a function of electric field of tunnel oxide with Pt gate during program operation. J_{back} boosting is not observed. Similar results are also obtained for Al, Mo and Au, as well.

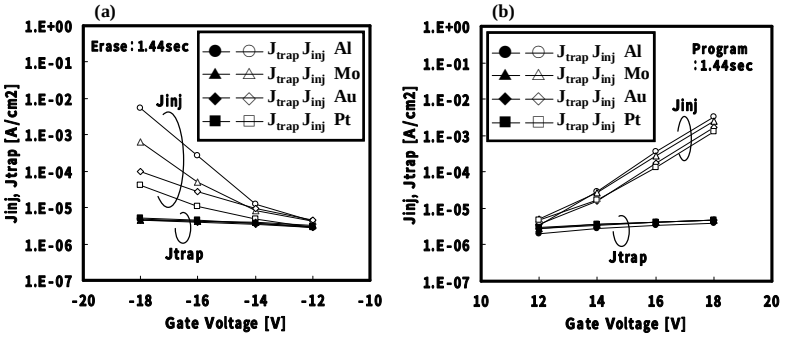

Fig.9 J_{inj} and J_{trap} as a function of applied voltage during (a) erase operation and (b) program operation.