Direct Measurement of Back-Tunneling Current during Program/Erase Operation of MONOS Memories and Its Dependence on Gate Work Function

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Introduction
MONOS memory is one of the candidates to replace floating gate (FG) non-volatile memory with its simple structure and less cell-to-cell interference [1]. Although multi-level cell operation is expected in MONOS memories to realize high density data storage, leakage current and back-tunneling current during program/erase (P/E) operation bring about Vth saturation [2] and narrow Vth window. Besides, it is known that penetration current severely degrades device reliability [3]. Thus, it is necessary to analyze current components of MONOS devices. Based on the charge-centroid extraction method [4][5], we have developed an analysis method which enables extracting back tunneling current component. In this paper, gate work function dependence of back-tunneling current during P/E operation is discussed to confirm the validity of our analysis scheme.

Analysis Method
The electrical distance of charge centroid \((z_{\text{eff}})\) from a gate electrode is derived as [4][5]:
\[
z_{\text{eff}} = -\varepsilon_o \Delta V_{\text{fb}} / Q_{\text{trap}}
\]
where \(Q_{\text{trap}}\) is the charge trapped in the nitride layer, \(\varepsilon_o\) is dielectric constant of SiO\(_2\) and \(\Delta V_{\text{fb}}\) is the flat-band voltage shift during P/E operation. To eliminate an error due to penetration current, \(z_{\text{eff}}\) is defined as a fixed value \((z_{\text{eff}}=0)\) once it is derived from a short time domain in P/E operation, thereby assuming 100% carrier capture efficiency. \(Q_{\text{trap}}\) is then derived in all time range as:
\[
Q_{\text{trap}} = -\varepsilon_o \Delta V_{\text{fb}} / z_{\text{eff}}
\]

Back Tunneling from Polysilicon Gate during Erase Operation
Fig.2 shows \(V_{\text{th}}\) shift as a function of time during erase operation of MONOS with n-poly-Si gate. Charge centroid \((z_{\text{eff}})\) extracted from a short time domain is located at around the SiN/Al\(2\)O\(_3\) interface, as depicted in the inset of Fig.2. Time evolutions of \(J_{\text{inj}}\) and \(J_{\text{trap}}\) are visualized in Fig.3. With increasing gate voltage, \(J_{\text{inj}}\) is boosted up and the trap efficiency \(J_{\text{trap}}/J_{\text{inj}}\) drops down deeper. The presence of back-tunneling current from the gate is evidenced when \(J_{\text{inj}}\) is plotted as a function of \(E_{\text{BLK}}\). As shown in Fig.4, \(J_{\text{inj}}\) appears as a unique and increasing function of \(E_{\text{BLK}}\). Hence we conclude that in MONOS devices with n-poly-Si gate, \(J_{\text{inj}}\) mainly consists of \(J_{\text{back}}\) during deep erase operation.

Metal Work-Function Dependence of Back Tunneling
1) Erase Operation
The dependence of back-tunneling current on the work function of metal gate electrodes (Al, Mo, Au and Pt) during erase operation is summarized in Figs.5 and 6. In this comparison, erase voltage and initial \(V_{\text{th}}\) are set to the same value for all metal electrodes. Time evolutions of \(J_{\text{inj}}\) and \(J_{\text{trap}}\) in Fig.5 indicate the increase of \(J_{\text{inj}}\) with a decrease of gate work function when entering into deep erase condition.

Fig.6 (a)-(d) shows \(J_{\text{inj}}\) and \(J_{\text{trap}}\) as a function of tunnel oxide electric field \(E_{\text{OX}}\) in a wide range of gate voltage (-12 ~ -18V). It is found that \(J_{\text{trap}}\)’s at different erase voltages form a common envelope curve corresponding to 100% carrier capture. It is also shown that \(J_{\text{inj}}\) at a low erase voltage (-12V) follow the envelope curve in all the metal gate materials. However, in Al gate, deviation of \(J_{\text{inj}}\) from the common curve is observed at higher erase voltages. The deviation of \(J_{\text{inj}}\) is only slightly observed for the highest erase voltage (-18V) in Mo gate. On the contrary, for the metal gates with even higher work function (Au and Pt), the deviation of \(J_{\text{inj}}\) is not observed at any erase voltage. The results indicate strong dependence of back tunneling current on the gate work function during deep erase operation.

2) Program Operation
Fig.7 shows \(J_{\text{inj}}\) as a function of time during program operation. Time evolution of \(J_{\text{inj}}\) is almost the same for all the gate materials, implying the absence of back tunneling current. This inference is confirmed by Fig.8 (\(J_{\text{inj}}\) vs. \(E_{\text{OX}}\)), showing no deviation of \(J_{\text{inj}}\) from a common envelope curve even for the gate electrode with a high work function (Pt). Hence it is concluded that back-tunneling current from the gate is negligible during deep program operation.

3) Comparison of \(J_{\text{inj}}\) and \(J_{\text{trap}}\)
The summary of currents during program/erase operation is depicted in Fig.9. Injected current \(J_{\text{inj}}\) is a increasing function of gate voltage. Strong dependence of \(J_{\text{inj}}\) on gate work function is obtained during erase operation. On the contrary there is negligible dependence of \(J_{\text{inj}}\) on gate work function.

Conclusions
In this work, we proposed a new analysis scheme to distinguish back-tunneling current from measured injected current on MONOS devices. It is found that in deep program/erase condition, leakage or back-tunneling current is the dominant component of \(J_{\text{inj}}\), respectively. Especially, \(J_{\text{back}}\) boosting is remarkable when using a gate electrode with low work function. In contrast, the dependence of \(J_{\text{trap}}\) on gate work function is found to be negligible. These results
give new information that is never obtained from analyzing $J_{trap}$ (or $V_{g-o}$) characteristics only. They will provide useful insight into reliability prediction of MONOS memories.

**Acknowledgement**

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![Fig.1 Current flow from Si-substrate ($J_{trap}$, $J_{back}$) and back-tunneling current from gate electrode ($J_{back}$) during erase operation.](image)

**Table 1 MONOS samples used in this paper.**

<table>
<thead>
<tr>
<th>#</th>
<th>Substrate</th>
<th>Tunnel oxide</th>
<th>Charge layer</th>
<th>Black oxide</th>
<th>Electrode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P</td>
<td>SiO2 4nm</td>
<td>Polysilicon</td>
<td>Al2O3 10nm</td>
<td>Pt</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
<td>SiO2 4nm</td>
<td>Polysilicon</td>
<td>Al2O3 10nm</td>
<td>Au</td>
</tr>
<tr>
<td>3</td>
<td>P</td>
<td>SiO2 4nm</td>
<td>Polysilicon</td>
<td>Al2O3 10nm</td>
<td>Mo</td>
</tr>
<tr>
<td>4</td>
<td>N</td>
<td>SiO2 4nm</td>
<td>Polysilicon</td>
<td>Al2O3 10nm</td>
<td>Pt</td>
</tr>
<tr>
<td>5</td>
<td>N</td>
<td>SiO2 4nm</td>
<td>Polysilicon</td>
<td>Al2O3 10nm</td>
<td>Au</td>
</tr>
<tr>
<td>6</td>
<td>N</td>
<td>SiO2 4nm</td>
<td>Polysilicon</td>
<td>Al2O3 10nm</td>
<td>Mo</td>
</tr>
</tbody>
</table>

Work function (eV) : Al(4.28), Mo(4.6), Au(5.1), Pt(5.65) from Herbert B. Michaelson, JAP 48, 4729 (1977).

![Fig.2 Erase characteristics of MONOS device with n-poly silicon gate. The charge centroid is located around the SiN/Al2O3 interface (inset).](image)

**Fig.4 $J_{mj}$ as a function of electric field of block oxide. $J_{back}$ boosting is observed.**

![Fig.3 $J_{trap}$ and $J_{mj}$ extracted from erase operation of sample #1. $J_{mj}$ boosting suggests back-tunneling current from gate electrode.](image)

**Fig.5 Work function dependence of $J_{mj}$ during erase operation.**

![Fig.6 $J_{mj}$ as a function of tunnel oxide electric field during erase operation with (a)Al gate, (b)Mo gate, (c)Au gate and (d)Pt gate. $J_{back}$ boosting is observed when using Al gate.](image)

**Fig.8 $J_{mj}$ as a function of electric field of tunnel oxide with Pt gate during program operation. $J_{back}$ boosting is not observed. Similar results are also obtained for Al, Mo and Au, as well.**

![Fig.9 $J_{mj}$ and $J_{trap}$ as a function of applied voltage during (a) erase operation and (b) program operation.](image)

**References**