Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp859-860

Thickness Effect on Read Window in a Two-Bit Nitrided-Based Trapping Storage Cell

G. D. Lee, C. H. Cheng, S. H. Ku, C. H. Liu, S. H. Kuo, C. H. Lee, S. W. Huang, N. K. Zous, M. S. Chen, W. P. Lu, K. C. Chen and Chih-Yuan Lu

Macronix International Co., Ltd, No. 16, Li-Hsin Road, Science Park, Hsin-Chu, Taiwan, R.O.C
Phone: +886-3-5786688-78160 E-mail : gdlee@mxic.com.tw, andersonliu@mxic.com.tw

Abstract

The read window, which is mainly determined by the 2nd bit effect, has been studied in respect to various ONO thickness combinations of a SONOS cell. The read window is increased with increasing top oxide thickness (Tox) but degrades as thickening the bottom oxide thickness (Box). A rectangular charge with a fixed width is employed to emulate the 2nd bit effect. Surprisingly, the lateral distribution of the trapped charge induced surface potential variation is found to be different for different thickness combinations even when their peak surface potentials are kept. To minimize such field spreading, thinning down Box is required. Finally, an improved read window has been successfully demonstrated on a 65nm product based on our work.

Introduction

Channel hot electron injection, which emits the charge in a localized region to the trapping medium of a SONOS device, is used as a programming method to provide the capability to store two bits per cell and the basic principle of 2-bit operation is described in [1]. Ideally, there is no interaction between the two bits in a cell. However, cross talk has been identified in [2], named as 2nd effect (complimentary bit disturb in [3]). This effect will induce read window saturation [4] and gets worse as channel length scales [3]. Thus, suppressing the 2nd bit effect becomes a must. Reference [3] also reports that such effect will depend on the ONO thickness but they simply explain by a different cell programming speed. In this work, we try to study the thickness dependence on the 2nd bit effect more detailed by incorporating both experiments and simulations. Cells with W/L=0.065/0.1 μm are used and the condition of thickness combinations, which use in device characterizations, simulation, and product measurements, are listed in Table I.

Experiments and Results

In Fig. 1(a), experiment procedures are shown. Firstly, the drain side of a cell is programmed. A source bias is then applied to read out the V_T status of the first programmed bit (bit 1). The V_T status of the neighbor bit within a same cell is also recorded by applying drain bias (bit 2). Increasing the reading V_D or Vs can minimize the 2nd bit but enhance read disturb, as shown in Fig. 2(a) and (b). Here, 1.6V of reading bias is chosen. The program and read procedure is continued until the V_T of bit 1 reaches a certain level. The results are plotted in Fig. 3(a) and Fig. 4(a) for various thickness stacks. In Fig. 3(a), Tox is varied while Box is unchanged. Similar to reference [3], the 2nd bit gets better as increasing effective oxide thickness (EOT). However, in Fig. 3(b), the three curves tend to converge together when their EOTs are normalized. This implies that the difference mainly comes from the EOT difference in these Tox split. But the EOT difference seems not the only factor to affect the 2nd bit effect. In Fig. 4(a), two samples have a similar EOT but the thickness of top and bottom oxide is exchanged. The 2nd bit effect increased drastically once the bottom oxide gets thicker. In Fig. 4(b), the read window is plotted and it is found that the window becomes smaller for a thicker bottom oxide. In addition, read window gets saturation because the increasing ΔV_T is compensated by 2nd bit effect.

Since cells with different EOTs are used, the programmed charge density and the programmed charge width will be different for each case. It is hard to identify which factor is the dominant one to lead to such experiment results. Therefore, a 2D simulation is employed in the following to help us find out the key factor behinds.

Simulation and Discussion

A schematic diagram for simulation is illustrated in Fig. 1(b). Charges with 20nm width are placed in SiN film above the junction edge and half of them are extended to the channel area. With changing the charge density, 2nd bit behavior and silicon surface potential were extracted. Following such procedure, the correlation between ONO thickness and electrical behavior could also be analyzed. Fig. 5(a) shows the 2nd bit effect under different ONO thickness and Fig. 5(b) re-plots them by normalizing to their own EOT. Comparing with Fig. 3 and Fig. 4, the simulated results emulate the experimental results very well. It should be emphasized that the width of trapped charges remains unchanged for all cases. This suggests that the charge width are not responsible for the observed phenomena. To understand what the root cause is, the surface potential along the channel direction are plotted for these ONO stacks in Fig. 6. In Fig. 6(a), the applied V_Gs are equal to their intrinsic V_T (V_{TI}) and Vs=1.6V. The stored charges of each case are carefully chosen to have an identical peak surface potential, implying the similar ΔV_T after programming bit 1. From the figure, different lateral spreading of the surface potential is clearly noted. A thicker bottom oxide shows a wider potential distribution caused by trapped charge. In other words, a thinner bottom oxide has a better field controllability over the channel region and thus obtains a narrow potential distribution even when all cases have the same width of stored charges (=20nm). Although increasing the Tox tends to have a wider lateral potential distribution, the impact is not as obvious as increasing Box (control and case B in Fig. 6(b)). As to 2nd bit effect, $V_G=V_{TI}$ and V_D=1.6V are applied and a significant difference in peak potential is observed. The cell with thinnest Box has a lowest peak, thus a slightest 2nd bit effect. Besides 2nd bit effect, gate disturb caused by program gate bias should also be considered during Box scaling. When bit 1 is programmed, the gate disturb, which is performed at V_G=11V for 2s, is increasing with decreasing Box and the maximum net window locates at Box= (O1-1.8nm). The performances of net read window are compared in Fig. 8 for control and case E. 16WLs are involved in the test and half of them are programmed. During program, a checkerboard pattern is chosen to maximize the 2nd bit effect. Since EOT is nearly identical for the two cases, similar initial and program distribution are found in Fig.8. As expected, a noticeable improvement is obtained for the V_T distribution of 2nd bit of case E.

Conclusion

We had demonstrated that the 2nd bit effect of a two-bit nitrided-based trapping storage cell is not only correlated to EOT but also affected by the ratio between Box and Tox. Field controllability of trapped charges over the lateral direction has been identified as an important factor. Thus, thinner Box along with thicker Tox leads to improved read window in voltage. Product data reveals that 1.8nm oxide exchange from Tox to Box results in 8.5% total window improvement.

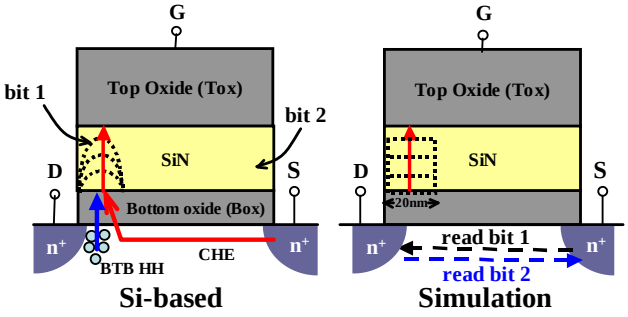

Fig.1 Schematic representation of the cell structure with two-bit storage. CHE and BTB HH injection are used for program and erase, respectively. A reverse read scheme is adopted for two-bit sensing. A rectangular charge with 20nm width is used for charge storage simulation

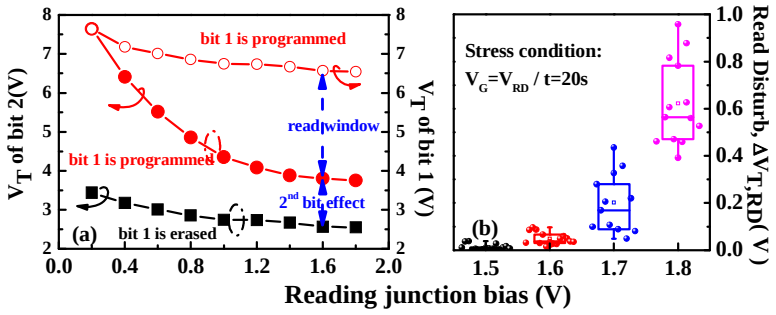

Fig.2 (a) Read junction bias effect on the reverse scheme. (b) Read disturb gets worse with increasing junction bias. Junction bias=1.6V is selected.

Table. 1 Sample descriptions. Three splits are compared. First is the Tox thickness split. Second is the exchanged Tox and Box thickness but keeps EOT. Third is our golden condition.

split / thickness	Control	Case A	Case B	Case C	Case D	Case E
Box	O1	O1	O1	O2 + 11 nm	O1 - 3 nm	O1 – 1.8nm
SiN	SiN	SiN	SiN	SiN	SiN	SiN
Tox	O2	O2 + 20 nm	O2 + 11 nm	O1	O2 + 14 nm	O2 + 1.8nm

Tox split

fixed EOT

fixed EOT to control

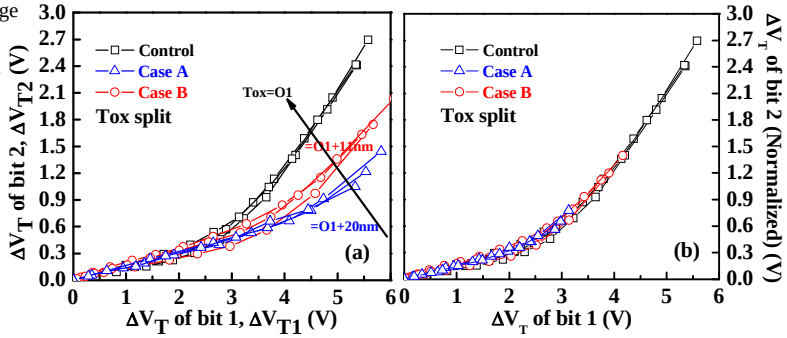

Fig.3 Measured 2nd bit effect for different Tox. (a) w/o, (b) w/ normalized by EOT.

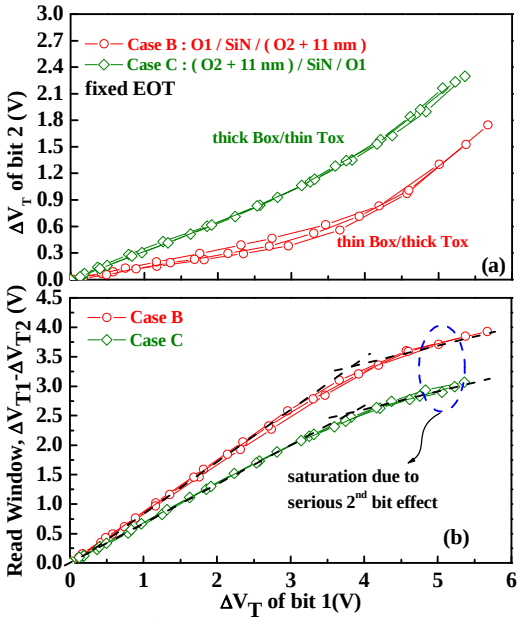

Fig.4 Measured 2nd bit effect for two devices with exchanged Tox and Box (EOT is kept). (b) Read window of Fig. 4(a).

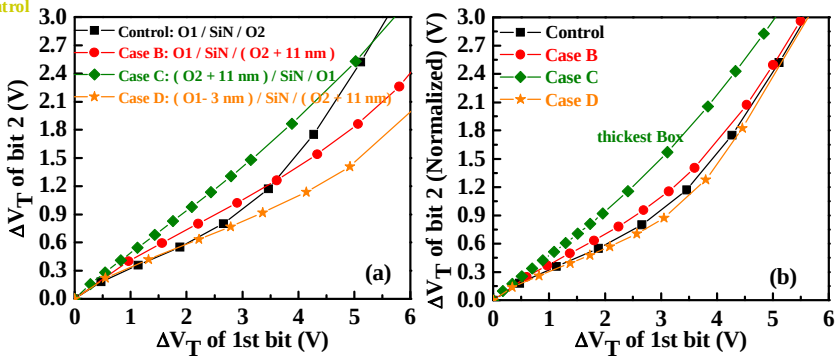

Fig.5 Simulated 2nd bit effect for various cases. (a) w/o, (b) w/ normalized by EOT.

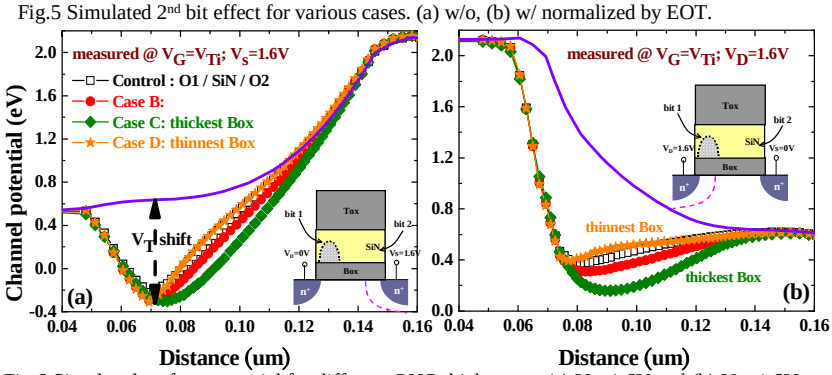

Fig.6 Simulated surface potential for different ONO thickness at (a) Vs=1.6V and (b) V_D=1.6V

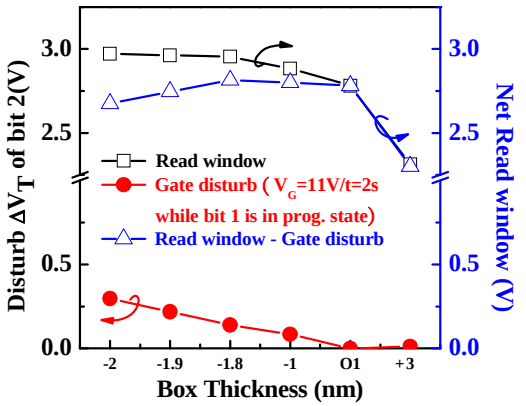

Fig.7 Bottom oxide thickness effect on the net read window (read window-gate disturb). EOT is kept in this study.

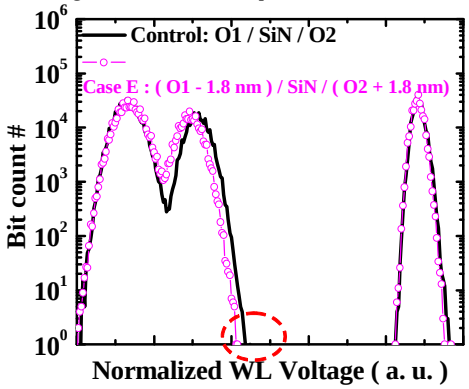

Fig.8 Measured V_T distribution of a 65nm product. The read window of case E has a 8.5% larger as compared to control sample.

Reference

[1] B. Eitan et al., in IEEE EDL., Vol.21, p.543-545, 2000

[2] Y. W. Chang et al., in IEEE EDL., Vol.25, p. 95-97, 2004

[3] L. Wang et al., in ICSICT., p.766-768, 2006

[4] L. Perniola et al., in IEEE TED., Vol.4, p.360-368, 2005