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Engineering of Si-rich Nitride Charge-Trapping Layer for Highly Reliable MONOS Type NAND Flash Memory with MLC Operation

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Abstract

The relationship between chemical structure (N/Si ratio) or physical structure (laminate structure) of Si-rich nitride charge-trapping layer for MONOS and its electrical characteristics (Program/Erase window, fresh data retention and data retention after Program/Erase cycling stress) are investigated in detail. A laminate structure of Si-rich nitride has been developed that can realize a sufficient Program/Erase window and excellent data retention for MLC operation.

1. Introduction

Charge-trapping type non-volatile memory, such as MONOS, has attracted increasing attention owing to its less cell-to-cell interference than the conventional Floating Gate (FG) type NAND Flash memory [1,2]. However, it is difficult to simultaneously satisfy a sufficient memory window for multi-level cell (MLC) operation (mainly because of the poor erase performance) and high reliability [3].

Si-rich nitride (SRN) charge-trapping layer is well known to be a promising approach for improving the Program/Erase (P/E) window [4,5]. However, the exact relation between the SRN film structure and cell characteristics including reliability has not been well understood.

In this work, we intensively investigated the relation between the chemical bonding structure or physical structure of charge-trapping SRN film and electrical characteristics in terms of P/E window and data retention (fresh and after P/E cycling stress). We also demonstrated the SRN engineering that enables a sufficient P/E window and excellent data retention (DR) for MLC operation to be obtained.

2. Experimental

The MONOS capacitor with n+ diffusion layer on p-type Si substrate was fabricated as shown in Fig.1 (a). Fig.1 (b) shows the cross-sectional TEM image of the MONOS stack. The tunnel oxide (5nm) was thermally grown, and the charge-trapping SRN (5nm) was deposited by ALD method using dichlorosilane (DCS) and NH_3. Then, the composition (N/Si ratio) of SRN was modulated by controlling the DCS/NH_3 gas supply ratio. After that, the blocking Al_2O_3 layer (15nm) and TaN/n+ poly-Si gate electrode were formed.

Fig.2 shows the schematic diagrams of the charge-trapping SRN structures formed in our experiment. Fig.2 (A)-(D) shows single SRN layer with varying N/Si ratio from 1.23 to 1.07, and Fig.2 (E)-(H) shows laminate structure composed of N/Si=1.23 and N/Si=1.07 SRN. The total thickness of laminated SRN was set to 5nm.

3. Results and Discussion

At first, the effect of varying N/Si ratio of single SRN charge-trapping layer on the electrical characteristics is investigated in detail.

Fig.3 shows the Si2p XPS spectra of silicon nitride films with varying N/Si ratio. The chemical shift attributed to Si-Si bonds clearly increases, with a decrease in N/Si ratio.

The P/E characteristics of fabricated MONOS capacitors for single SRN layer are shown in Fig.4 (a) and (b), respectively. The P/E window increase as N/Si ratio decreases, and SRN with N/Si ratio of less than 1.09 has a sufficient P/E window for MLC operation. It must be noted that only the erase speed gets faster with a decrease in N/Si ratio. It indicates that electron trap property at program operation is independent of the SRN bulk condition, which implies electrons are trapped only at the interface between SRN and Al_2O_3 as reported previously [6,7]. In contrast, the erase characteristic is determined by the SRN bulk condition. The Si-richer SRN seems to have shallower traps and larger electron mobility due to the excess Si-Si bonds. Therefore, the trapped electrons at the upper interface easily move to the bottom side and detrap to the substrate at erase operation.

Fig.5 shows the DR characteristics (program ΔVfb shift) of fresh and after P/E cycling stress at 85℃. The fresh DR was degraded with a decrease in N/Si ratio. It is likely that the degradation of fresh DR is also caused by the excess Si-Si bonds (electron moving toward the bottom interface and detrap to the substrate), because we have confirmed that fresh DR is improved when the tunnel oxide gets thicker (not shown).

On the other hand, DR after P/E cycling stress was improved with a decrease in N/Si ratio. Then, the P/E cycling was performed at constant P/E window width, and two widths of window were performed. For N/Si=1.23, there is no DR data for the wider window due to the poor endurance characteristics. Fig.6 shows the correlation between ΔVfb shifts due to DR after P/E cycling stress and erase voltage that was applied during P/E cycling. It is found that ΔVfb shifts depend absolutely on the erase voltage regardless of the chemical bonding structure of SRN film. In other words, DR after P/E cycling stress is mainly determined by the erase performance. It is thought that the main cause of degradation of DR after P/E cycling stress is penetration of high-energy back-tunneling electron from gate electrode to the substrate at high erase voltage, as illustrated in the energy band diagram of Fig.7.

From these results, an increase of Si content in single SRN layer improves the erase speed due to the excess Si-Si bonds, and it induces the improvement of after cycling stress DR. However, it simultaneously causes the degradation of fresh DR.

On the other hand, it is found that the laminate SRN is effective structure to overcome the trade-off. It can suppress the electron moving during fresh data retention as well as keeping high electron detrap efficiency at erase operation, as discussed below.

Fig.8 shows the P/E speed of some samples shown in Fig.2 (Fig.2 (A), (D) and (E) to (H)). The P/E speed was represented by ΔVfb by applying a certain program or erase pulse. As in the case of Fig.4, only the erase speed is strongly affected by the SRN structure. Among the laminated samples, relatively fast erase was obtained in laminate (E) and (H). Both are effective structures to enhance the electron detrap at erase operation, because the N/Si=1.07 layer is relatively thick and located just upon or close to the tunnel oxide.

Fig.9 shows the fresh and after P/E cycling stress (wide window) DR characteristics at 85℃. The poor fresh DR of single Si-richer SRN (D) was certainly improved by forming the laminate structure, especially in laminate (F), (G) and (H). A certain degree of thickness of N/Si=1.23 layer seems to be necessary (at least 2nm) to suppress the moving of electron toward the bottom interface during retention. On the other hand, the lower ΔVfb shifts of after cycling DR were obtained with the laminate (E) and (H). As expected, it strongly correlates with the erase speed.

The result shows that the charge-trapping SRN structure (H) is the optimum one to simultaneously satisfy the P/E window for MLC operation and DR both of fresh and after P/E cycling.

4. Conclusion

The effect of charge-trapping SRN engineering (N/Si ratio and laminate structure) on electrical characteristics was clearly demonstrated. The developed laminate SRN structure allows a sufficient P/E window and excellent DR characteristic (both of fresh and after P/E cycling stress) for MLC operation to be obtained. It is effective structure for suppressing the electron moving in the charge-trapping layer during fresh data retention, as well as keeping high electron detrap efficiency at erase operation.

References

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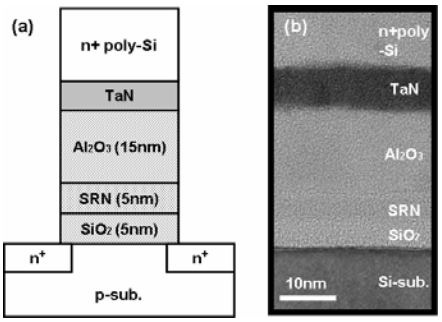

Fig.1 (a) Schematic diagram and (b) Cross-sectional TEM image of fabricated MONOS capacitor

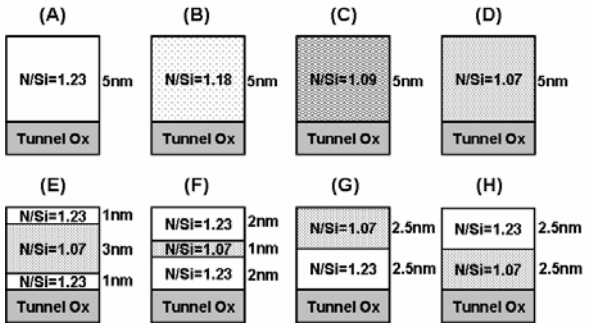

Fig.2 Schematic diagrams of charge-trapping SRN layer

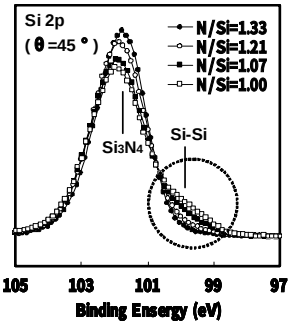

Fig.3 Si 2p XPS spectra of SiN films with varying N/Si ratio

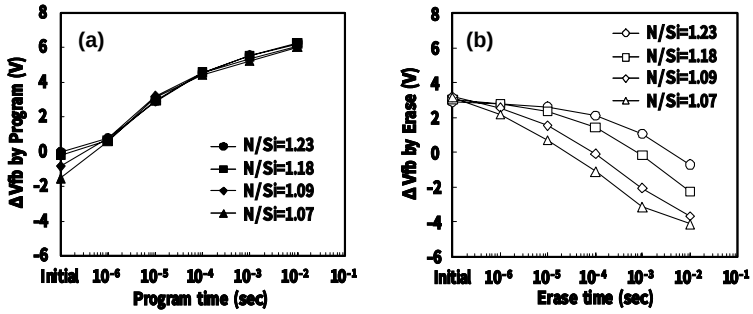

Fig.4 (a) Program and (b) Erase characteristics of MONOS capacitor with varying N/Si ratio of single SRN charge trapping layer

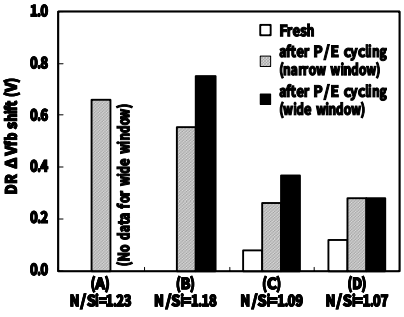

Fig.5 Data retention characteristics of fresh and after P/E cycling stress at 85℃

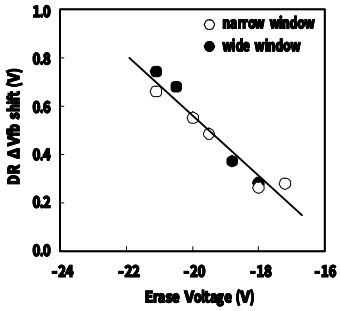

Fig.6 Correlation between ΔVfb shifts of data retention after P/E cycling stress and erase voltage that was applied during P/E cycling

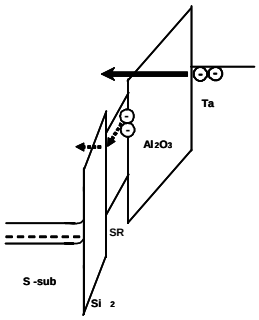

Fig.7 Energy band diagram of MONOS stack when high erase voltage was applied

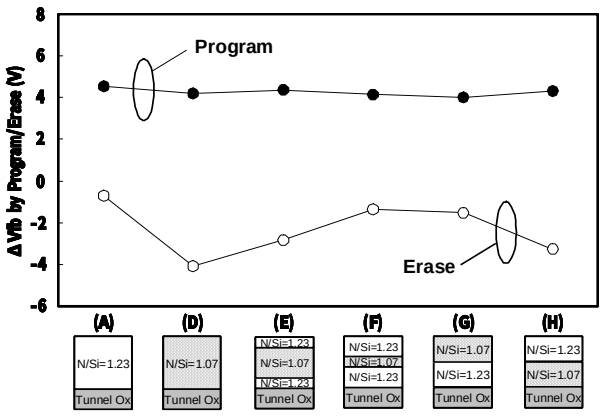

Fig.8 Program and erase speed of laminated charge-trapping layer

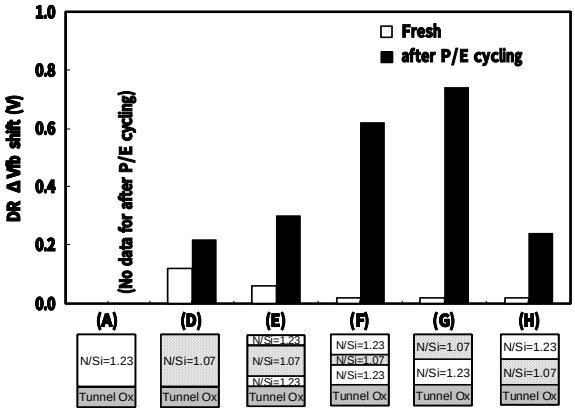

Fig.9 Data retention characteristics of fresh and after P/E cycling stress at 85℃ of laminated charge-trapping layer