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Depletion-type Cell-Transistor of 23 nm Cell Size on Partial SOI Substrate for NAND Flash Memory

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1. Abstract

To reduce the short channel effect for memory cell transistors beyond 2Xnm cell size for NAND Flash memories, we propose a depletion-type cell transistor fabricated on a self-manufactured partial SOI substrate by conventional LSI process and solid phase epitaxy. The memory cell transistors with stack-gate show well program / erase properties and have the typical S-factor of 366mV/decay. Short channel effect is reduced substantially to available level for 2Xnm size NAND Flash memory.

2. Introduction

A planner-type NAND Flash Memory which is fabricated by conventional LSI process and operates at multi-level cell (MLC) mode is demanded also beyond 2X nm cell size. As the channel length become shorter, the short channel effect of the cell transistor causes turn-off problem [1], which is problem for the NAND Flash memory under MLC mode of operation. To eliminate the problem we propose a **D**epletion-type cell-**T**ransistor **o**n a **P**artial **S**OI-substrate (D-ToPS) for NAND Flash memory. Source / channel / drain regions of the D-ToPS are doped with the same impurity (non p-n junction) in a unit cell, and the depletion layer which expands wider than the gate length stretches out below the gate oxide to cut-off a cell current, therefore short channel effect can be reduced substantially.

3. Process and Fabrication

The scheme of the process of D-ToPS is shown in Fig. 1. SiO_2 layer on Si substrate is partially etched off to make patterned opening (a). Amorphous Si is deposited on the SiO_2 layer (b). The amorphous Si is changed to single crystal Si (SOI) by solid phase epitaxy (SPE) (c). N-type impurity is implanted in SOI source / channel / drain regions. Sequential process between tunnel oxide deposition and stack-gate fabrication is almost the same as conventional floating gate NAND Flash memory (d). All these steps are conventional Si based process.

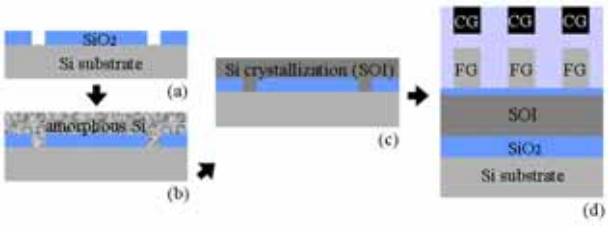

Fig. 1 Schematic process flow of the D-ToPS for NAND Flash memory

Cross-sectional TEM images for the D-ToPS for NAND Flash memory are shown in Fig.2. The channel measures 23nm in length and 23nm in width.

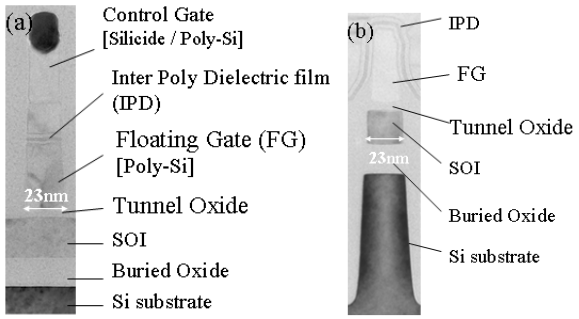

Fig. 2 Cross-sectional TEM image for D-ToPS for NAND Flash memory of gate length of 23nm (a) and gate width of 23nm (b)

The SPE growth TEM images on the various direction Si substrates are shown in Fig.3. Poly Si is grown on the Si (111) seed region (a) and single crystalline Si (c-Si) is grown on the Si (100) seed region (b). Lateral SPE growth speed to <100> direction is faster than <110> direction (b) and (c).

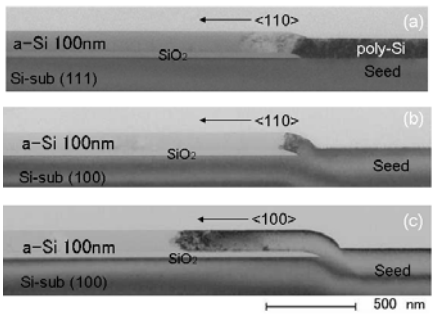

Fig.3 Cross-sectional TEM Image for SPE growth on the various direction Si substrates.

The J-E characteristics of thermal SiO_2 on the c-Si SOI and the partial poly-Si SOI by SPE growth in Fig. 4. The brake down electric-field of SiO_2 on the c-Si SOI is higher than that on the partial poly-Si SOI and the low electric-filed hump of c-Si SOI J-E curve is reduced. In this reason, Si (100) substrate and <100> lateral growth direction is selected for this D-ToPs technology.

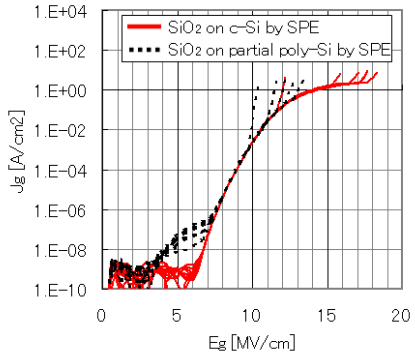

Fig. 4 J-E characteristics of dielectric on the single crystalline and the partial polycrystalline SPE Si

4. Operation Principle

The operation principle of the D-ToPS for NAND Flash memory is illustrated in Fig. 4. A depletion layer stretches out from the surface of n-SOI channel region and current path is pinched off (a), when a certain quantity of electrons are stored in a floating-gate. On the other hand, applying positive gate bias, the depletion layer reduces and then the channel turns on (b). Program and erase operations are applying positive bias to gate electrode and substrate (SOI), respectively. Since the depletion layer which expands wider than the gate length stretches out below the gate oxide, short channel effect can be reduced substantially.

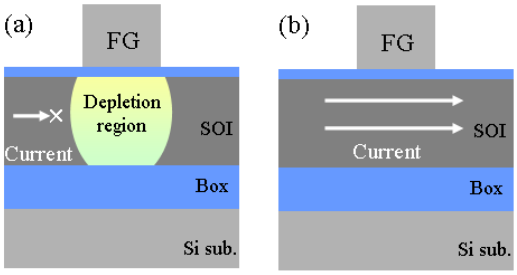

Fig. 4 Operation principle of the D-ToPS for NAND Flash memory Turn-off mode (a) and Turn-on mode (b)

5. Results and Discussions

Typical I-V characteristics are shown in Fig. 5. The S-factor is 366 mV/decay. These excellent characteristics of high cell current and small S-factor are essential to realize MLC mode of operation. Program and erase characteristics are shown in Fig. 6 and Fig. 7. The program voltage and time for reaching a Vth of 5V are 23V and 100us, respectively, while the erase voltage and time for a Vth of -3V are 18V and 10us, respectively. These applied voltages of around 20V are usable range of a conventional NAND Flash memory peripheral circuit. Furthermore, measured Vth window of 16V between program and erase state is wide enough, and measured program and erase time of 100us and 10us are fast enough NAND Flash memory. And we observed slight narrowing of Vth-window and increase in Vth of about 1V after 1000 cycling test.

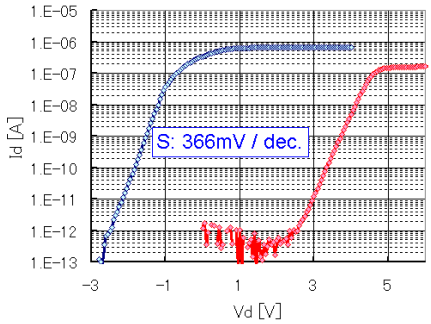

Fig. 5 Typical I-V characteristics of neutral cell (blue) and programmed cell (red)

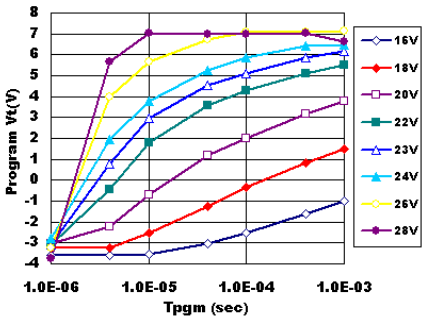

Fig. 6 Program characteristics varied program voltage between 16V and 28V

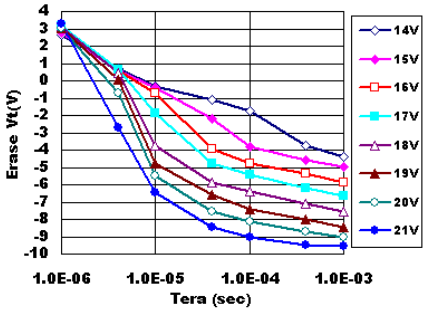

Fig. 7 Erase characteristics varied erase voltage between 14V and 21V

6. Conclusions

D-ToPS for NAND Flash memory reduces the short channel effect substantially to available level for beyond 2Xnm size NAND Flash memory. D-ToPS for NAND Flash memory of 23nm cell size is demonstrated with excellent device performances which are high enough cell current, small enough S-factor, wide enough Vth window and fast enough program / erase time. D-ToPS is fabricated by using just conventional Si based process. Applied bias sets of the program voltage and the erase voltage are almost the same range of that of conventional stack-gate NAND Flash memory. This D-ToPS for NAND Flash memory is probably applied beyond 2Xnm cell size without any design change of peripheral circuits.

Reference

[1] K. Inoh, Symposium on VLSI Technology, short course, 2007