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The Operation Scheme and Process Optimization in TLC(Triple Level Cell) NAND Flash Characteristics

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Abstract

As NAND flash market demand for larger capacity at low cost increases, the feature-size scaling and multi-level per bit have been developed. In this paper, we present the characteristics of NAND TLC (Triple Level Cell) performance and some operation schemes uniquely adopted in NAND TLC technology. And also the results of process experiments for improving its distribution, E/W cycle and retention characteristics are described.

1. Introduction

In order to achieve the larger capacity of NAND flash, a method of having more levels per cell, such as TLC, is being developed since the introduction of MLC concept [1]. In TLC NAND Flash, the 8 levels of Vth should be placed, which makes the device window narrow. For this reason, the newly adopted operation schemes such as interference cancellation and dynamic read are introduced, and optimized cell doping concentrations, mechanical stress reduction and heat treatment are also necessary.

2. Operation Scheme

Dynamic read scheme and Interference cancellation

The cell Vth distributions in TLC NAND flash should be tightly controlled since it has more cell levels than MLC. To position the 7 levels above zero volts, powerful ECC for treating the tail bits and dynamic reading scheme are essential as shown in Fig.1. It is, however, very difficult to guarantee the margins between the levels. Fig.2 shows dynamic read and interference cancellation schemes adopted in TLC for overcoming these obstacles. In the dynamic read scheme, read voltage is adjusted to a level where the number of fail bits of neighboring levels is minimized. Besides a controller chip which functions interference cancellation also compensates the Vth shift caused by neighboring F/G having various states.

Improved Program / Verification Scheme

To narrow the Vth distribution, the increment step of ISPP (Increasing Step Pulse Program) should be minimized. However, it degrades the program performance. Fig. 3(a) shows intelligent program scheme in which the starting program voltage of current (i th) page is determined from the program of previous (i-1 th) page. The other is blind verification program scheme. In this method, the upper level (n+1 th) is programmed without verifying, and the verification in the upper level is initiated after the lower level(n th) is programmed, which reduces the verifying time.

3. Experiments and Results

Cell Vth Distributions

In addition to the new operation algorithm, W/L dimension and doping concentration of cell transistor should be optimized for the cell Vth distribution. The variations in W/L dimension have a big influence on the program speed and so result in programmed Vth variations as shown in Fig.4. Another degrading factor is the doping concentration of cell channel which affects the hot carrier injection in edge W/L. F/G doping and grain structure also induce abnormally programmed cells [2] as shown in Fig.5.

E/W Cycles

Fig.6 shows that the failed block portions increase as E/W cycles. The trapped charge affects the S/D overlap with gate, hence the S/D concentration should be optimized. And also the space from cell active to C/G should be controlled to reduce the electric field during E/W operation.

Retention

It is impossible to avoid changes in mechanical stress during thin film and annealing process. The tensile stress type of a passivation layer has improved characteristics as shown in Fig.7 [3]. And the retention characteristics are related with the mobile charges migrated from neighboring materials. Fig. 8 shows the charge loss due to mobile charges accounts for major portion among total charge loss [4]. Hence it is important to understand the source of mobile charges during fabrication and assembly process.

Read Disturbance

In TLC operation, the read voltage is higher than MLC. Fig.9 shows that the increased read voltage of 8V induces the electron injection into F/G of erased cell, which causes the erased cell failure. It is, therefore, essential to reduce the read bias through tight Vth distributions or placing the levels in negative Vth region.

4. Conclusions

In this paper, the newly adopted dynamic read, interference cancellation, improved program/verification schemes are described for TLC operation. In terms of process conditions, uniformity in cell dimensions, cell doping concentration, mechanical stress in thin film and suppressing the mobile charges are discussed to control the tight Vth and reliability characteristics.

References

[1] M. Bauer, et al., ISSCC, pp.132-133, 1995
[2] H. Miki, et al., IEEE IRPS, pp 29-35, 2007
[3] R. Arghavani, et al, IEEE Transactions on Electon Devices, Vol. 54, No. 2, Feb. 2007
[4] J. Liou et al., 6th International Symposium on PID, 2001.

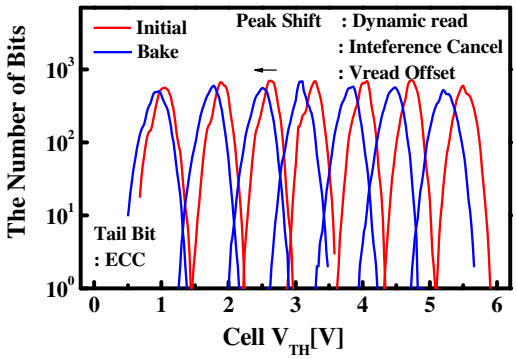

Fig.1 Actual program Vth distributions in Triple Level Cell (TLC, x3) before and after bake test.

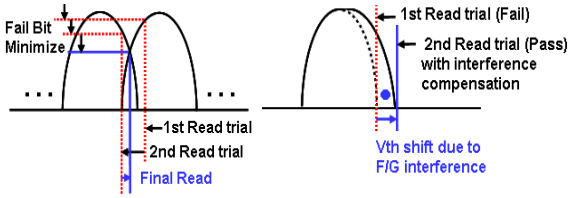

Fig.2 (a) Dynamic read scheme and (b) interference cancellation scheme by controller chip. These enable the stable read operation even in overlapped distributions.

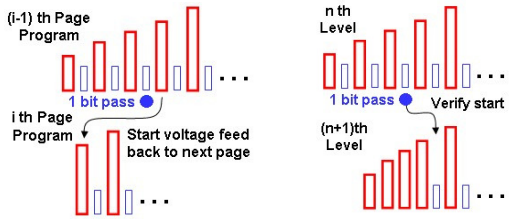

Fig.3 Newly adopted program and verification for programming performance in TLC. (a) Intelligent program start bias control scheme (b) Smart blind verification

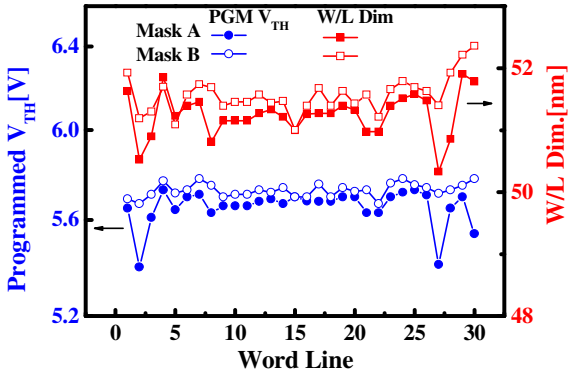

Fig.4 Programmed Vth of the individual W/Ls with various dimensions. W/L uniformity is essential for cell Vth distribution.

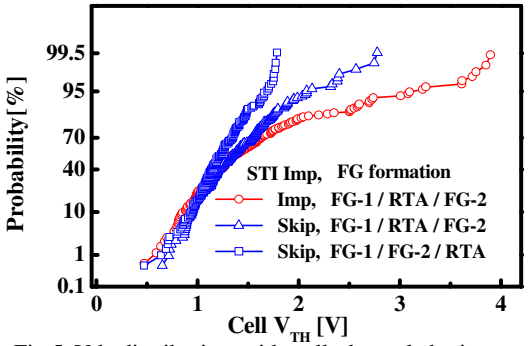

Fig.5 Vth distribution with cell channel doping and FG structure. Doping also influences the Vth distribution.

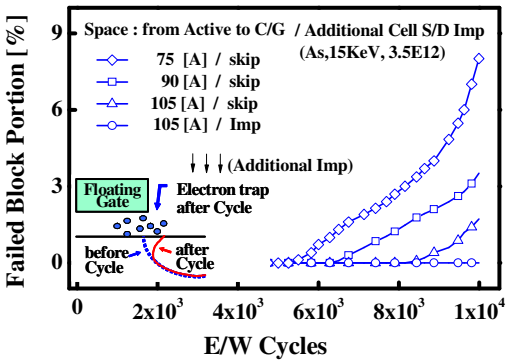

Fig. 6 The failed block portions after E/W cycling. E/W characteristics are affected by cell S/D concentration and space (electric field) between cell active and control gate during E/W cycles.

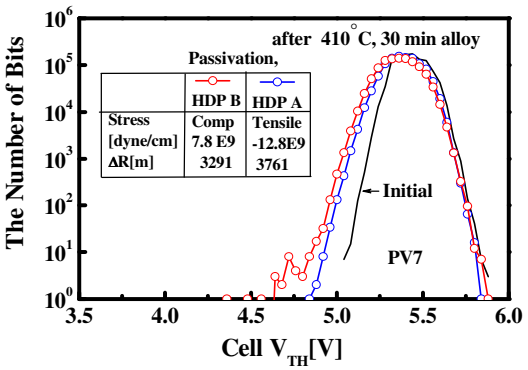

Fig.7 Retention characteristics with passivation films. The tensile stressed film has improved distribution after bake 150C, 24 hours..

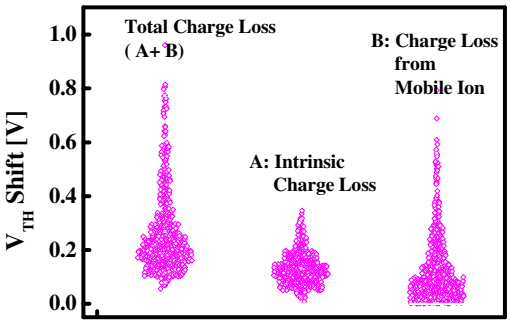

Fig. 8 Vth shift portion due to mobile ions and intrinsic charge loss. The charge loss portion of mobile ions is major portion.

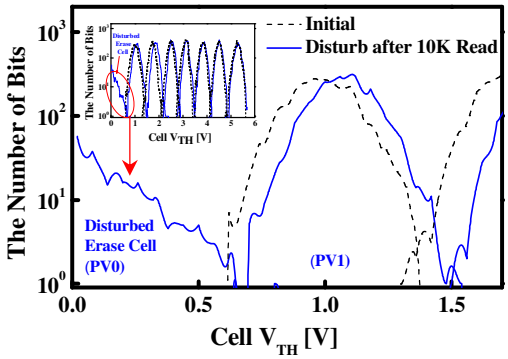

Fig. 9 Read disturbances after 10K read stress with a read bias of 8 V. The disturbances in erased levels are more severe due to FN injection.