The Influence of Mechanical Stress on Data Retention in Advanced NAND Flash

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Abstract

As the advance of NAND Flash technology, the small and unique geometry of cell structure is getting sensitive to process changes that were considered less importantly before. Although many articles warned the influence of mechanical stress on the reliability of Flash memories, the influence keeps evolving and altering with technologies and cell structures. In this paper, we present how the mechanical stress affects the data retention characteristics of advanced NAND Flash, and which process steps we should carefully control to improve the characteristics.

1. Introduction

NAND Flash memory must store data without change for years even after E/W endurance cycles. Mechanical stress during wafer fabrication is known as one of factors having influence on data retention characteristics in various mechanisms [1][2]. We evaluate the impact of mechanical stress on NAND Flash in 48nm technology node (Fig.1), and we have found the major mechanism how the stress improves/deteriorates data retention characteristics.

2. Experiments and Results

We cannot avoid changes in mechanical stress during wafer fabrication processes mostly coming from thin film deposition and annealing process as shown in Fig. 2. As previous articles show, we can clearly see that data retention characteristics are influenced by the composition of passivation as shown in Fig. 3. We can monitor the changes in passivation material with measuring refractive index (R.I.). In this experiment, we vary N₂O gas with fixing NH₃ and SiH gases. Until R.I.=1.64, as we reduce R.I., data retention after 5K endurance cycle improves. However, we cannot observe any more improvement with R.I.=1.62.

Hydrogen concentration keeps dropping with lowering R.I., so if low hydrogen concentration is the main factor to improve data retention, we should observe continuous improvement until R.I.=1.62. On the contrary, the data retention matches well with lowering compressive mechanical stress, which stops decreasing at R.I.=1.64 (Fig. 4).

In order to clarify exact mechanism and the impact of different processes, we planed experiment as shown in Table I. Fig. 5 shows the mechanical stress changes in wafer with process steps of Group A, B and C. Fig. 6 shows the stress changes of Group D. The difference between Group C and D is only changing the process sequence between depositing SiON and H2N2 anneal. In Group A, we reduce HDP oxide thickness as we add P-TEOS layer so that we

can ignore another impact from thickness changes.

As shown in Fig. 7, regardless of materials and process sequence, we can observe that final stress on wafer correlates with data retention. In other words, we can improve data retention with more tensile stress than compressive stress.

There are two possible mechanisms for mechanical stress to affect data retention: 1) Change in effective electron tunneling conductivity and 2) Trap site generation. In order to confirm the first mechanism, we measure F-N characteristics with modifying mechanical stresses, but we cannot observe any changes.

Fig. 8 shows the relation between data retention and oxide charge $trap(1C/cm^2)$ in gate edge intensive pattern with actual channel length(48nm). We tested various types of test patterns including large area, STI edge intensive pattern and large channel length (1um) gate edge intensive pattern. We have gate re-oxidation process step to cure gate edge damage during process. If we skip the re-oxidation step, we have very short time(<10s) retention failure due to oxide defect at gate edge, and it shows 600mV shift for reference. Only with modifying mechanical stress, we can improve Vg shift from 460mV to 225mV.

Fig. 9 confirms above results with main chip data, and it shows the maximum program bias differences before and after 10 endurance cycles with Group C and D. Only with 10 endurance cycles, Group C(-250mV) degrades faster than Group D(-140mV), and i.e., the program speed of C becomes faster than that of D. The only difference between them is process sequence, but as shown at Fig. 5 and Fig. 6, the stresses on wafer are much different.

3. Conclusions

In NAND Flash, as shown in Fig. 1, gate edge and STI edge are exposed to different process steps in terms of mechanical stress. Because the 2^{nd} poly protects the stress from outside at STI edge, we cannot observe any impact. Based on our analysis results, mechanical stress induced trap generation is turned out to be the main cause of improving/degrading data retention. Unlike other observations, the impact is getting severe with shorter channel length, so we need to carefully consider modifying mechanical stress during wafer fabrication process in right direction with advancing technology nodes.

References

- [1] A. Hamada at al., IEEE TED Vol. 38, No. 4, April 1991.
- [2] X. Yang at al., Applied Physics Letters 88, 2006.



Fig 1. 48nm NAND Flash structure.



Fig 2. Mechanical stress trends in wafer fabrication processes.



Fig 3. Data retention : uncorrectable bit error rate (UBER) with passivation refractive index.



Fig 4. Passviation film stress and hydrogen concentration with regard to passivation refractive index.

Group	P-TEOS	HDP	SiON	H2N2 Anneal
А	×	0	0	×
В	0	0	0	0
С	×	0	0	0
D	×	0	\bullet	•

D : Change Process Sequence

H2N2 Anneal before depositing SiON film.



Fig 5. Mechanical stress applied to wafer with process steps, (-) stands for compressive stress, (+) stands for tensile stress.



Fig 6. Mechanical stress with difference process steps (Group D).



Fig 7. UBER and mechanical stress with processes.



Charge Trap, Vg shift after $1C/cm^2$ stress [mV]Fig 8. The relation between UBER and tunnel oxide charge trap (Vg shift) at gate intensive pattern.



Fig 9. ISPP(Increasing Step Pulse Program) maximum bias before and after 10 E/W endurance cycles with processes.